

PY-Note Block Diagram

Project Code: DP710
PCB(Raw Card): 1.0

PCB Layer Stackup

- L1:TOP
- L2:GND
- L3:Signal
- L4:PWR
- L5:Signal
- L6:Signal
- L7:GND
- L8:Signal
- L9:GND
- L10:BOTTOM

Battery Charger

BQ24780SRUYR 88	
INPUTS	OUTPUTS
DOCK_FWR20	M-BAT-PWR

System DC/DC

TPS51285BRUKR 90	
VINT20	VCC5M
VCC3M	VCC3M

CPU DC/DC

M: NCP81205MNTXG 91	
S: NCP81382MNTXG 92, 93, 94	
VINT20	VCCCPU/CORE
VCCSA	VCCGFX/CORE

VCCCPUIO

NB681GD-C623-Z 95	
VCC5M	VCCCPUIO
VCC1R0_SUS	

VCC1R0_SUS

TPS51362RVER 96	
VCC5M	VCC1R0_SUS
VCC1R2A/VCC0R6B	

VCC1R2A/VCC0R6B +SMDDR_VREF_DIMM

TPS51716RUKR 99	
VINT20	+SMDDR_VREF_DIMM
VCC0R6B	VCC1R2A

VCC1R8B

BD9B300MUV-E2 98	
VCC5M	VCC1R8B
VCC2R5A	

VCC2R5A

BD91364AMU-ZE2 100	
VCC5M	VCC2R5A
VCC0PC/VCC0PIO(44e)	

VCC0PC/VCC0PIO(44e)

NB681GD-C623-Z 101	
NB681GD-C623-Z 103	
VCC5M	VCC0PC
VCC0PIO	

VCCGTX (44e)

NCP81210MNTXG 102	
VINT20	VCCGTX

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TABLE: SYSTEM POWER STATE

Power state to be determined

Schematics Mark Definition

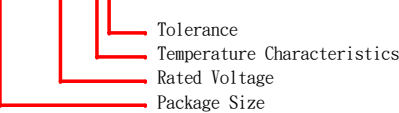
BOM Structure	4+2 CPU	4+4e CPU	Note
@	NO ASM	NO ASM	
EMC@	ASM	ASM	EMC
RF@	ASM	ASM	RF
ME@	ASM	ASM	ME
PRxxx, PCxxx, PLxxx	ASM	ASM	Power
42@	ASM	NO ASM	4+2 CPU
44e@	NO ASM	ASM	4+4e CPU

Any other mark like below is prohibited on Payton/Walter.
ESD@, EMI@, EMC_NS@, EMC_PX@, EMC_OPT@, CONN@,
CONN_NS@... RH, CH, LH(PCH related RLC)..

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX



Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+/-0.05PF	+/-0.1PF	+/-0.25PF	+/-0.5PF	+/-1%	+/-2%	+/-3%	+/-5%	+/-10%	+/-20%	+/-30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	+50, -20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

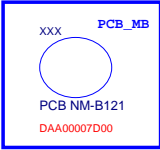
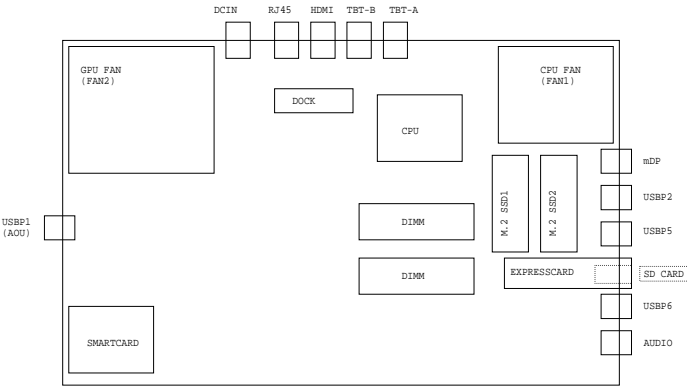
PCH SM Bus address

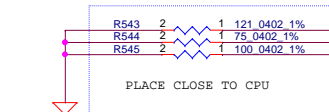
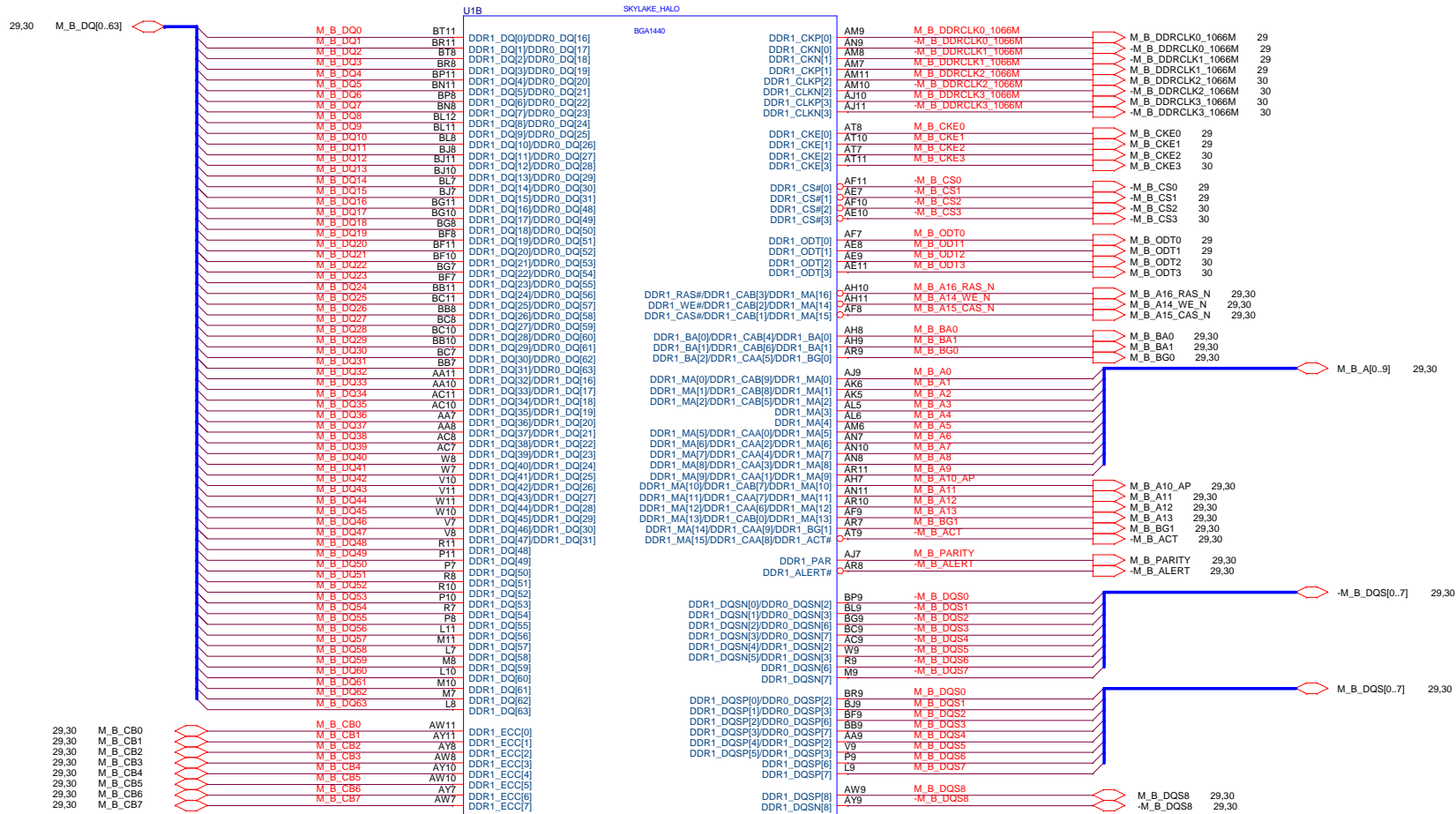
Device	Address
CH-A P DDR DIMM0	1001 0000b
CH-A S DDR DIMM1	1001 0001b
CH-B P DDR DIMM2	1001 0010b
CH-B S DDR DIMM3	1001 0011b

PCH SM Bus0 address



Device	Address
Intel Lan_I219	0XC8

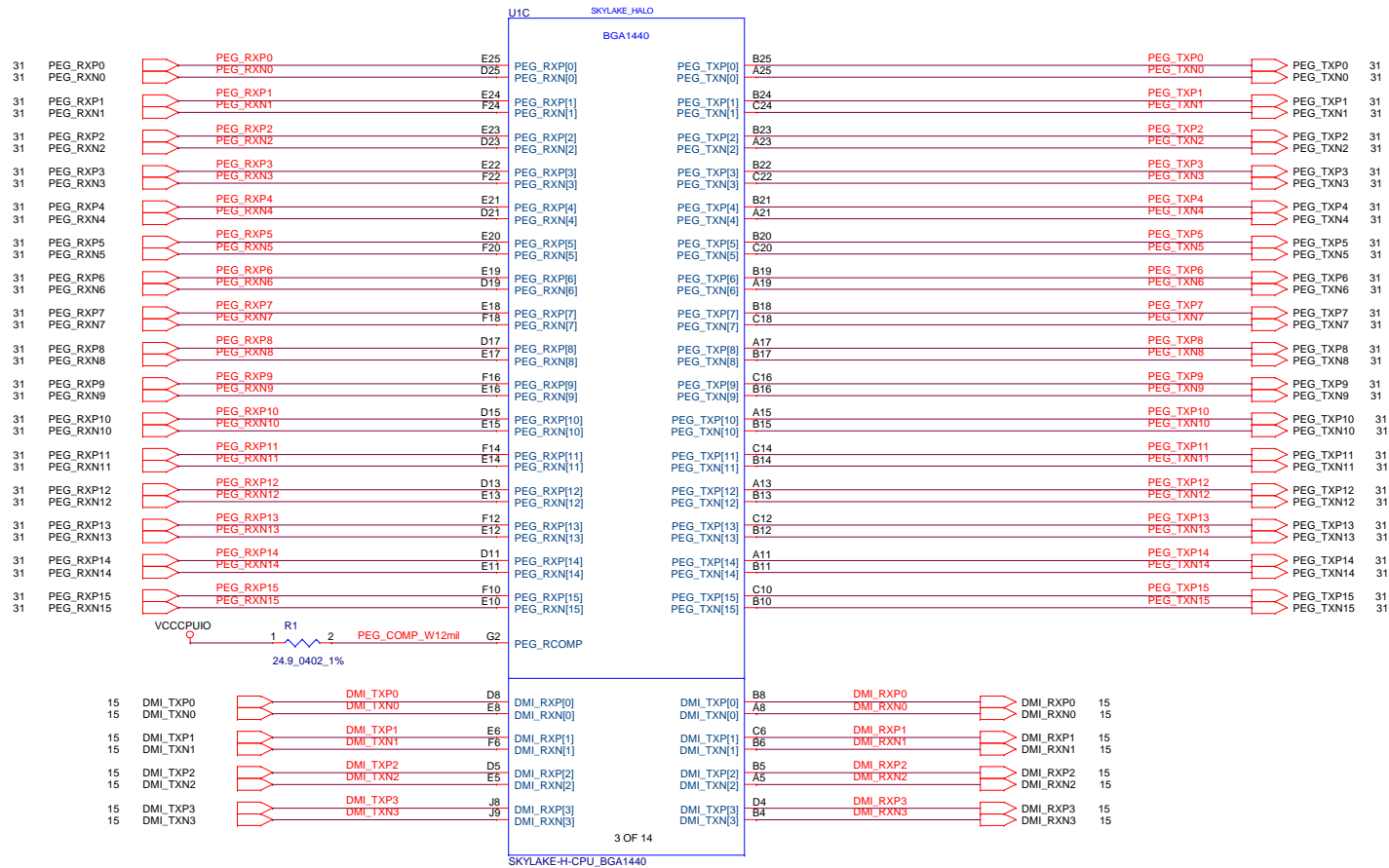
TABLE: SYSTEM COMPONENT PLACEMENT (AS OF 2014 Dec 8)

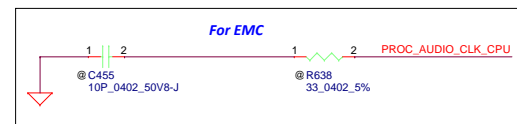
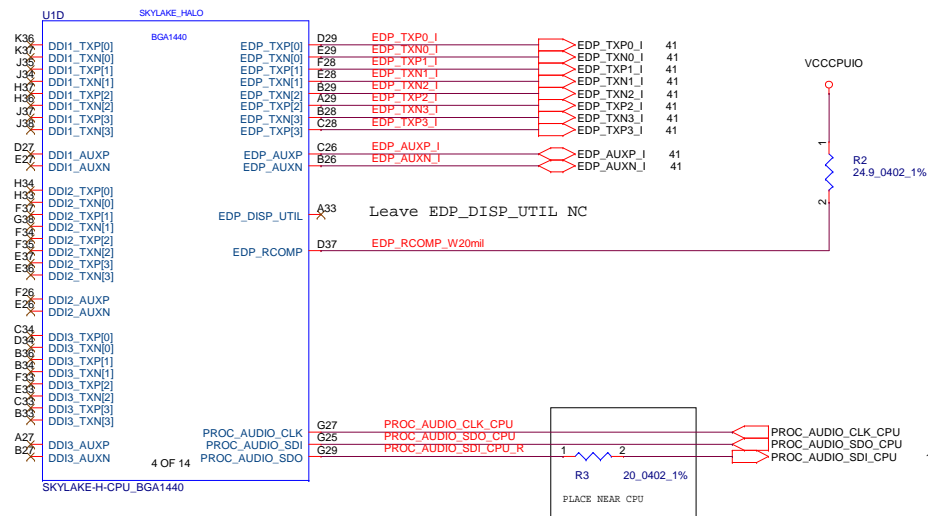





DDR_VREF_CA: Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ: NC
DDR1_VREF_DQ: Connected to VREF_CA on DIMM CH-B

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Issued Date	2015/07/16	Deciphered Date	2016/01/16	CPU SKL-H : DDR4 CH-B					
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PAYTON

U36	Supplier PN	LCFC PN
TI	SN74AUP1G07DCKR	SA00007F700
NXP	74AUP1G07GW	SA00007GU00

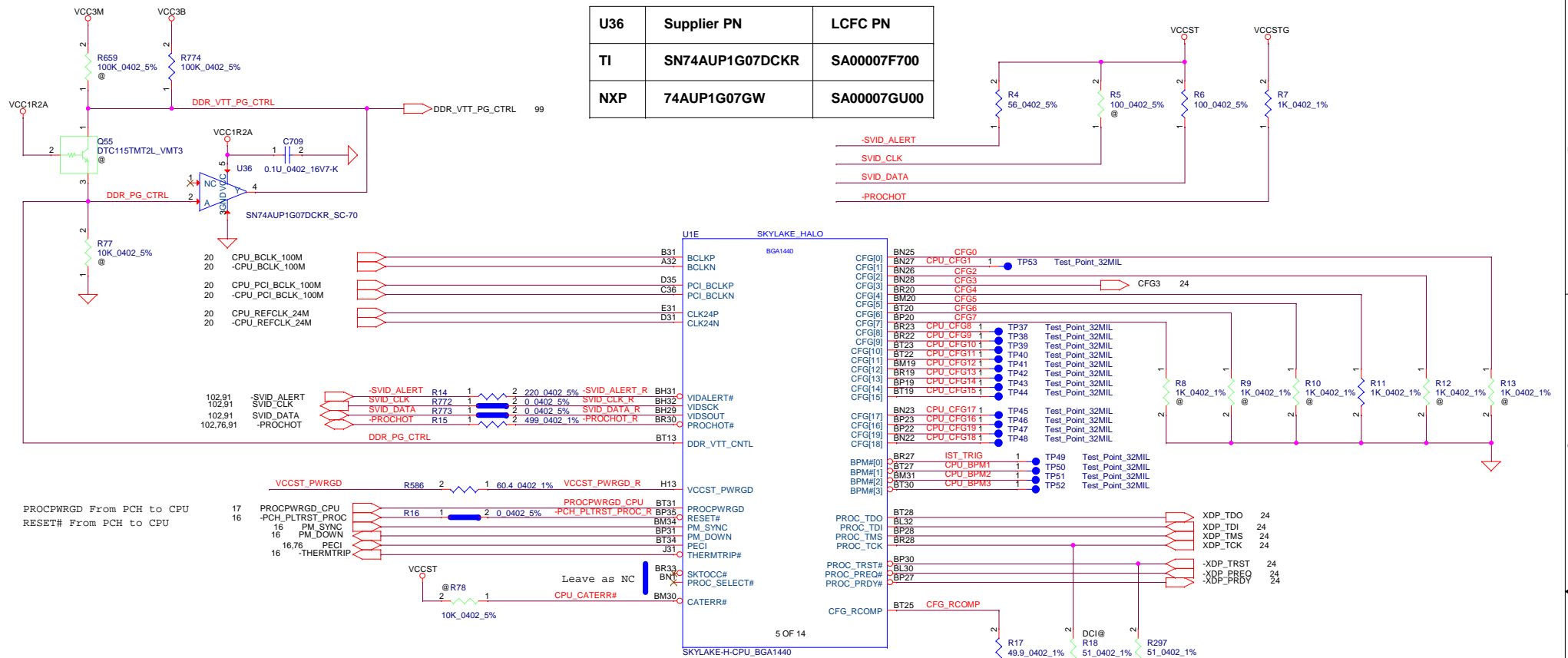


TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
 1 : No Stall ← LOGIC
 0 : Stall

CFG[2] : PEG Static Lane Reversal
 1 : Normal Operation ← LOGIC
 0 : Lane Reversal

CFG[4] : eDP enable
 1 : Disabled
 0 : Enabled ← LOGIC


CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0
 11 : 1x16 ← LOGIC

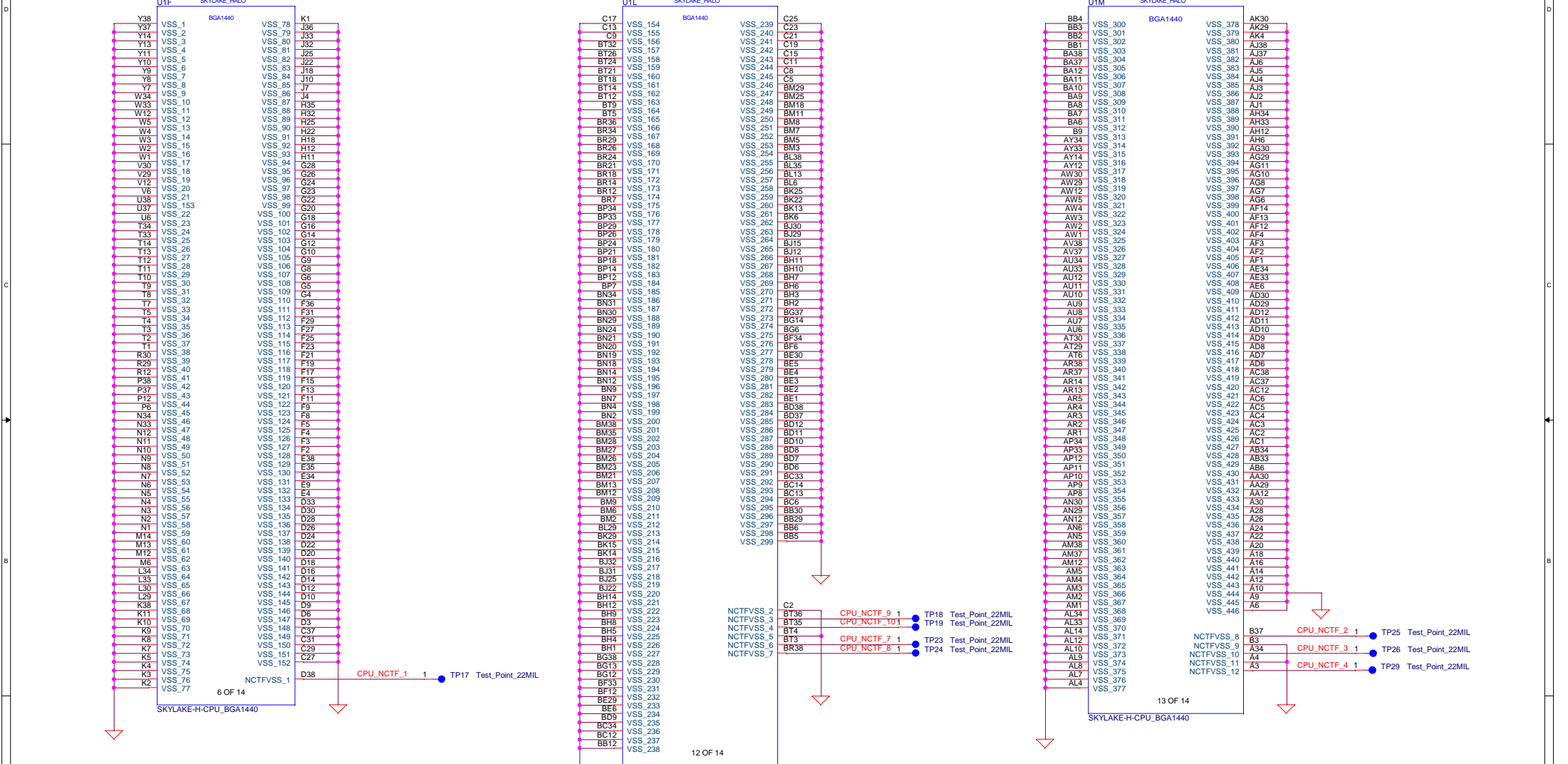
CFG[7] : PEG Training
 1 : PEG Train immediately following RESET# deassertion ← LOGIC
 0 : PEG Wait for BIOS for training

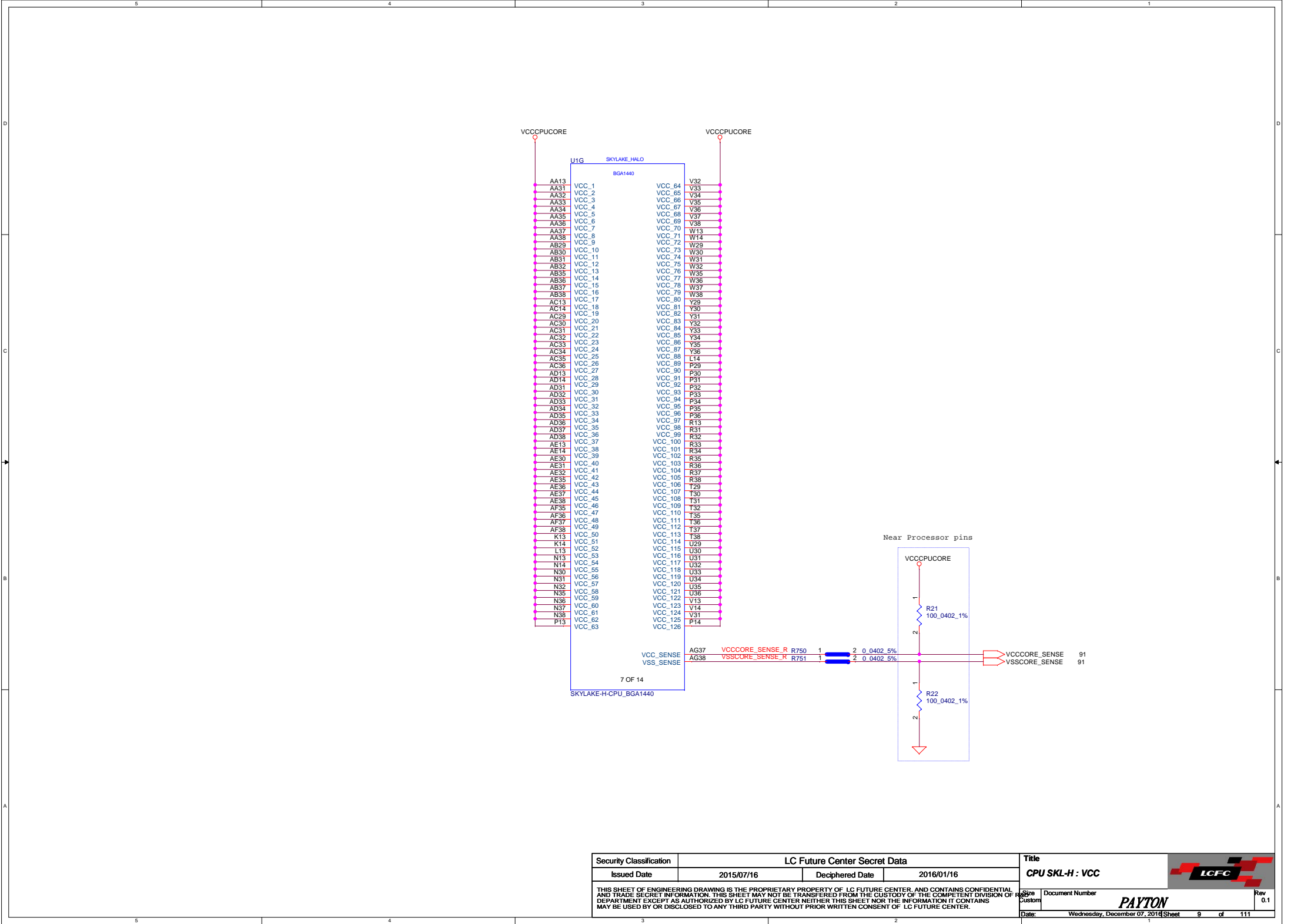
CFG[19:8] : Reserved

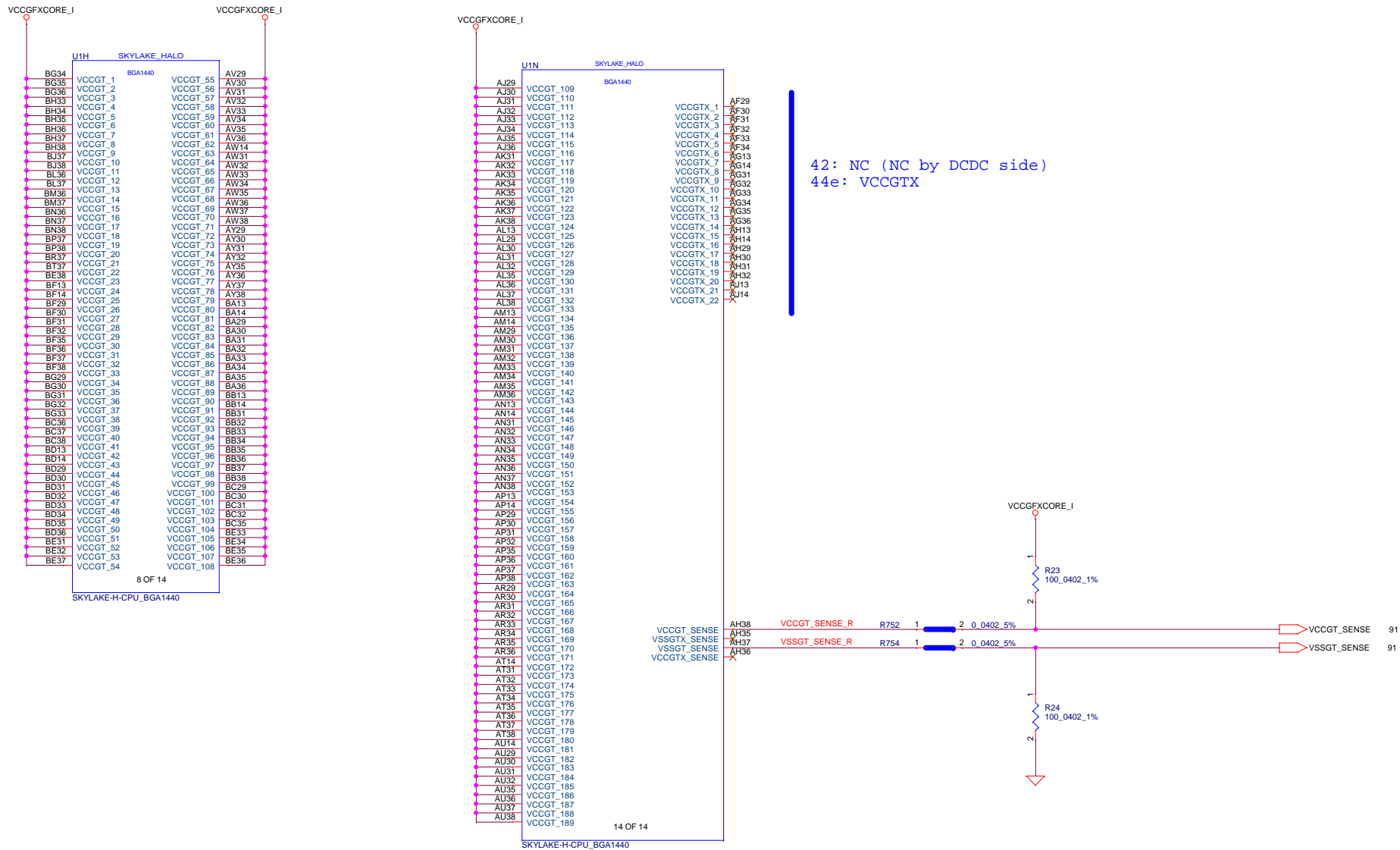
VCCST_PWRGD requirements (546884_SKL_H_PDG_Rev0_71)

- 1) Indication that the VCCST/VDDQ power supplies are stable and within specification. (Table 41-1)
- 2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST. (Figure 41-1 Note 1)
- 3) VCCST_PWRGD should be equal or earlier than PCH_PWROK. (Table 41-5, tCPU16. See also 543016_SKL_PDG_UY_1_0)
- 4) VCCST_PWRGD is typically made from ALL_SYS_PWRGD (CPUCORE_ON/VR_ON for CPU DCDC), not PCH_PWROK (CPUCORE_PWRGD). (Figure 41-1)

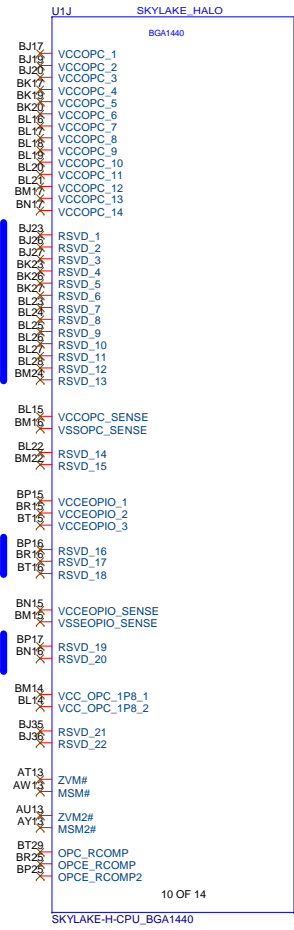
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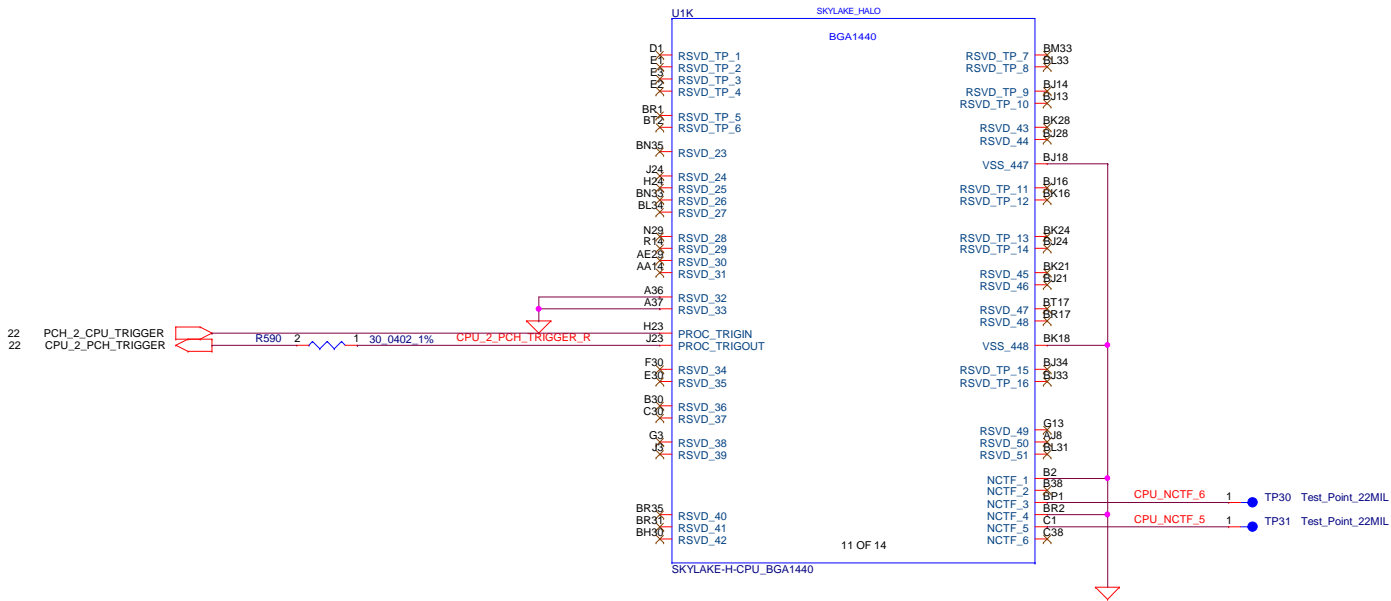


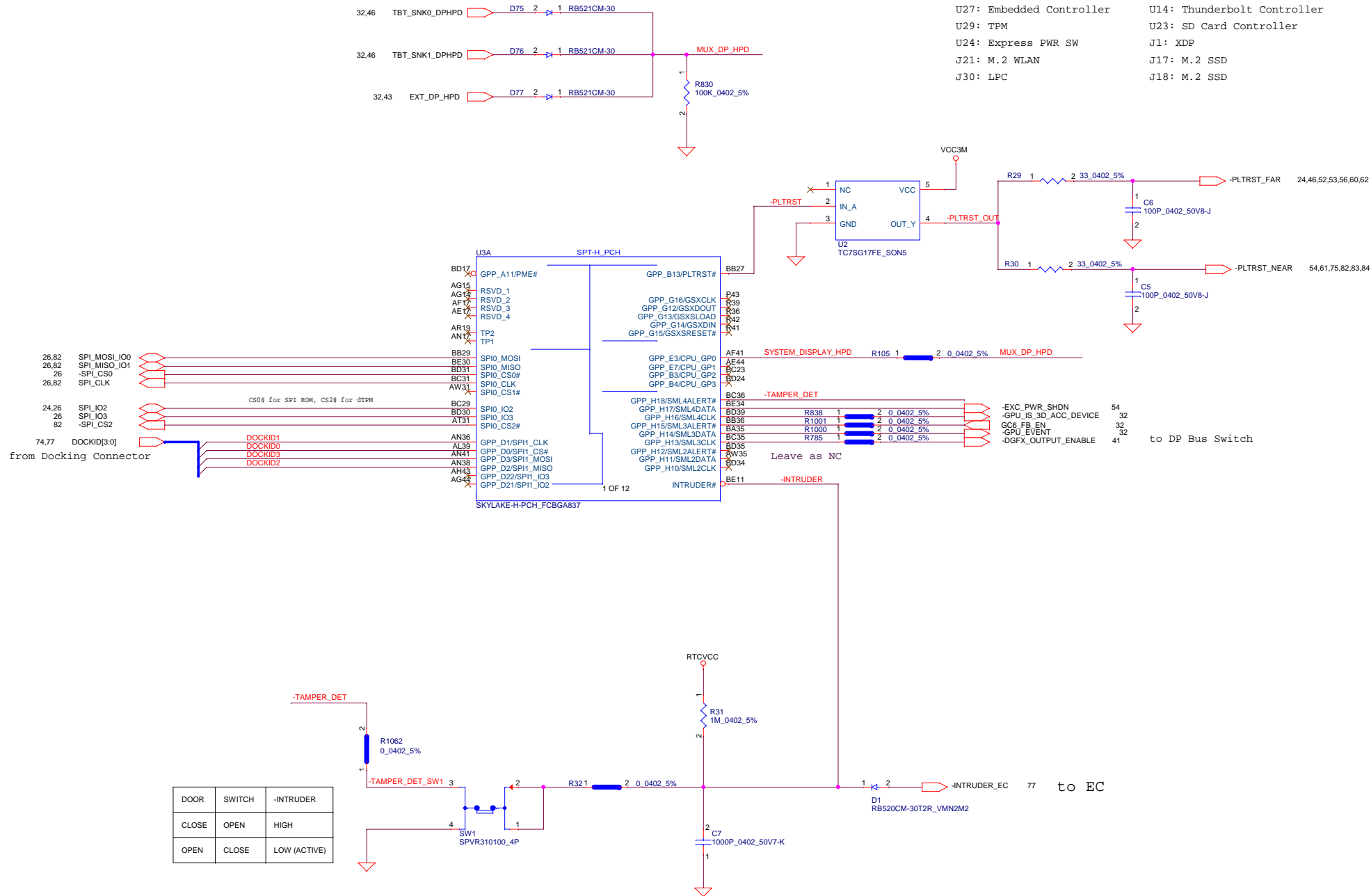




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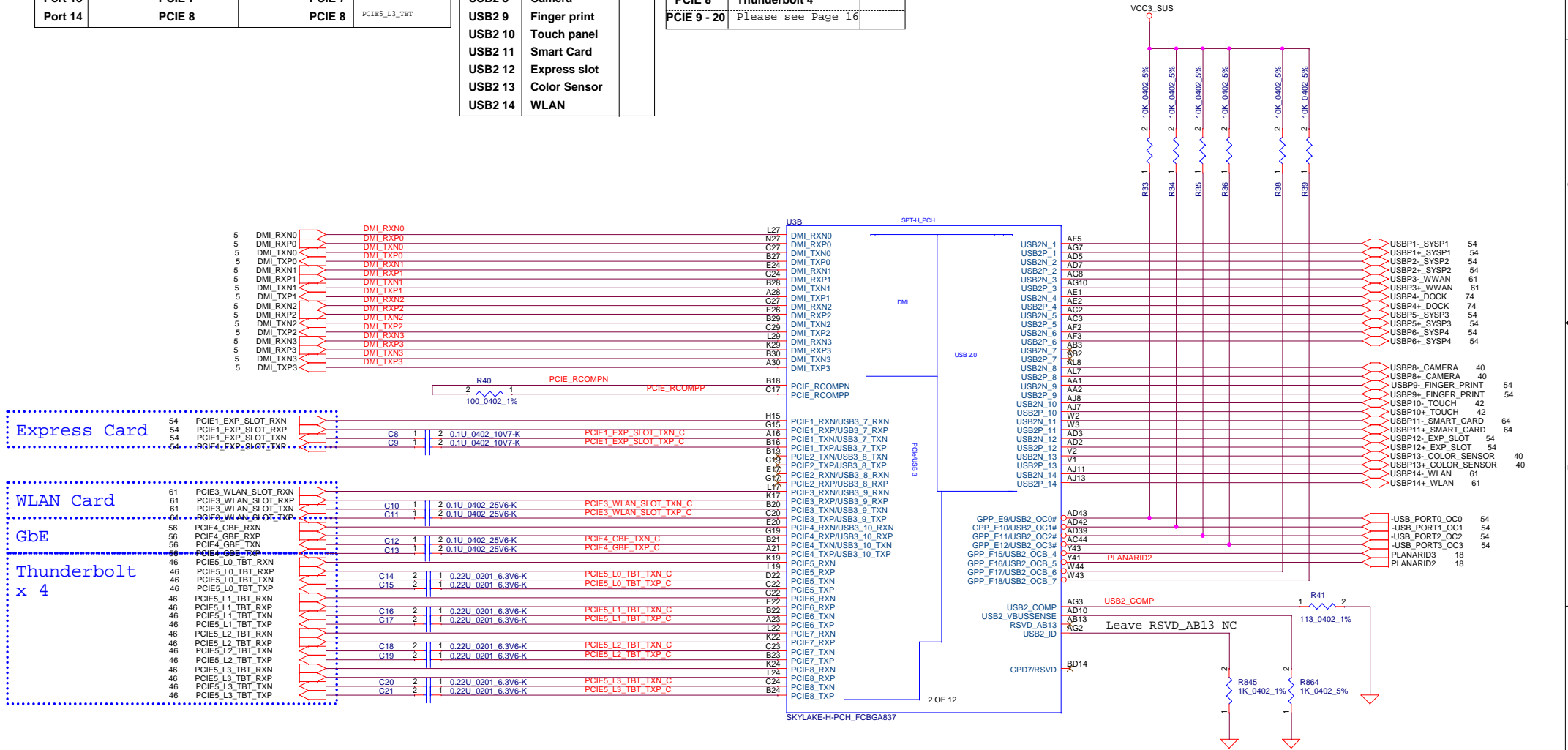


Flexible I/O Configuration (v0.51)			
I/O	High Speed Signals	Configuration	Net Name
Port 1 - 6		Please see Page 19	
Port 7	USB3 7 / PCIE 1	USB3 7 or PCIE 1	PCIE1_EXP_SLOT
Port 8	USB3 8 / PCIE 2	USB3 8	
Port 9	USB3 9 / PCIE 3	PCIE 3	PCIE3_WLAN_SLOT
Port 10	USB3 10 / PCIE 4 (GBE)	GBE	PCIE4_GBE
Port 11	PCIE 5 (GBE)	PCIE 5	PCIE5_L0_TBT
Port 12	PCIE 6	PCIE 6	PCIE5_L1_TBT
Port 13	PCIE 7	PCIE 7	PCIE5_L2_TBT
Port 14	PCIE 8	PCIE 8	PCIE5_L3_TBT

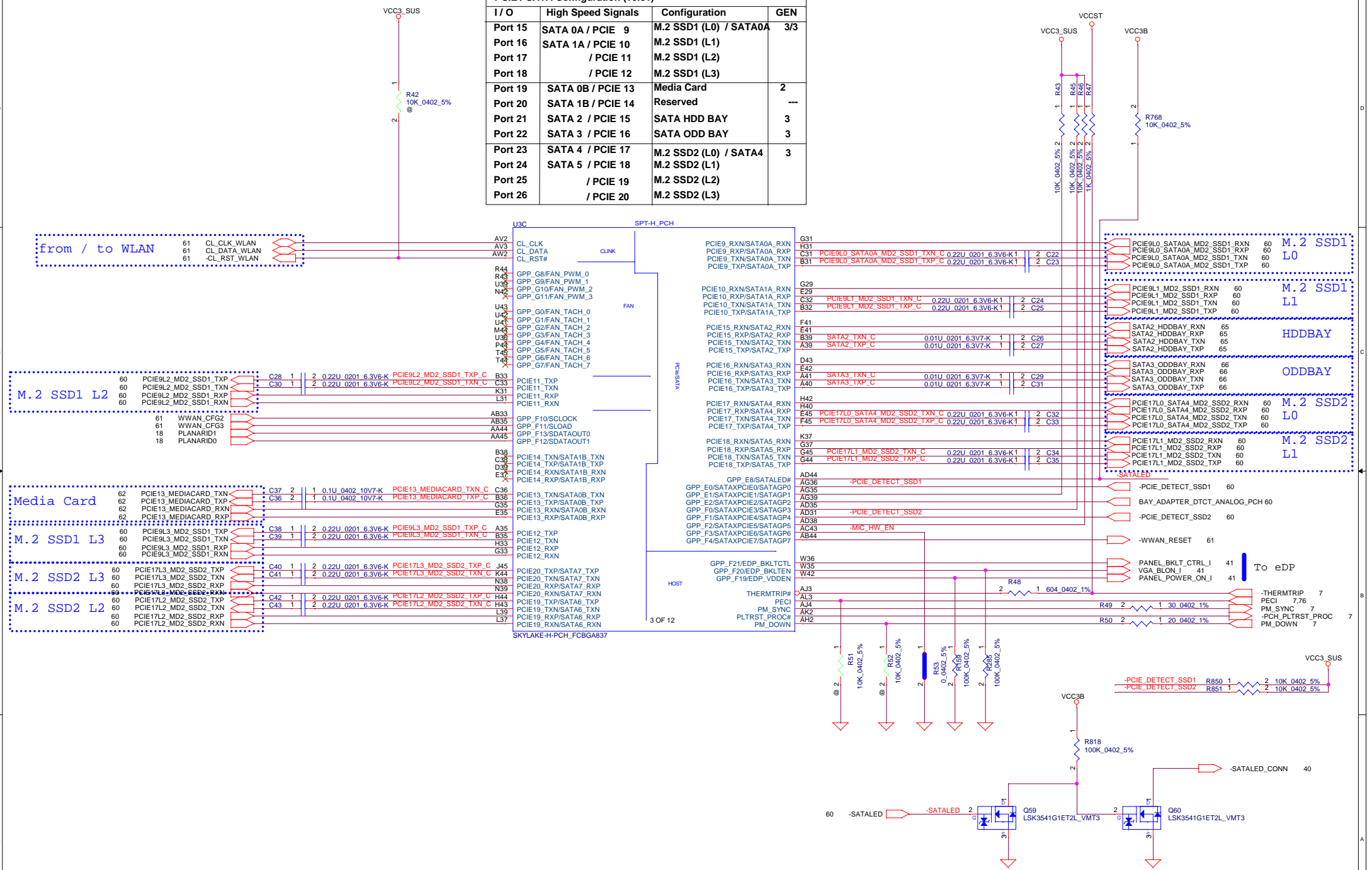
USB2.0 Configuration (v0.51)		
USB2 #	Assignment	OCx #
USB2 1	System Port 1	0
USB2 2	System Port 2	1
USB2 3	WWAN	
USB2 4	DOCK	
USB2 5	System Port 3	2
USB2 6	System Port 4	3
USB2 7	Reserved	
USB2 8	Camera	
USB2 9	Finger print	
USB2 10	Touch panel	
USB2 11	Smart Card	
USB2 12	Express slot	
USB2 13	Color Sensor	
USB2 14	WLAN	

PCIE Configuration (v0.51)		
PCIE #	High Speed Signals	GEN
PCIE 1	Express slot	2
PCIE 2		
PCIE 3	WLAN Card	2
PCIE 4	GBE	
PCIE 5	Thunderbolt 1	3
PCIE 6	Thunderbolt 2	
PCIE 7	Thunderbolt 3	
PCIE 8	Thunderbolt 4	
PCIE 9 - 20	Please see Page 16	

USB3.0 Configuration (v0.51)	
USB 3#	High Speed Signals
USB3 1 - 6	Please see Page 19
USB3 7	
USB3 8	
USB3 9	
USB3 10	



PCIE / SATA Configuration (v0.51)				
I / O	High Speed Signals	Configuration	GEN	
Port 15	SATA 0A / PCIE 9	M.2 SSD1 (L0) / SATA0A	3/3	
Port 16	SATA 1A / PCIE 10	M.2 SSD1 (L1)		
Port 17	/ PCIE 11	M.2 SSD1 (L2)		
Port 18	/ PCIE 12	M.2 SSD1 (L3)		
Port 19	SATA 0B / PCIE 13	Media Card	2	
Port 20	SATA 1B / PCIE 14	Reserved		
Port 21	SATA 2 / PCIE 15	SATA HDD BAY	3	
Port 22	SATA 3 / PCIE 16	SATA ODD BAY	3	
Port 23	SATA 4 / PCIE 17	M.2 SSD2 (L0) / SATA4	3	
Port 24	SATA 5 / PCIE 18	M.2 SSD2 (L1)		
Port 25	/ PCIE 19	M.2 SSD2 (L2)		
Port 26	/ PCIE 20	M.2 SSD2 (L3)		



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HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

PLACE ON BOTTOM SIDE

VCC3_SUS

1 R54 2
1K_0402_5%

1 R55 2
0_0402_5%

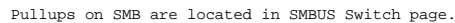
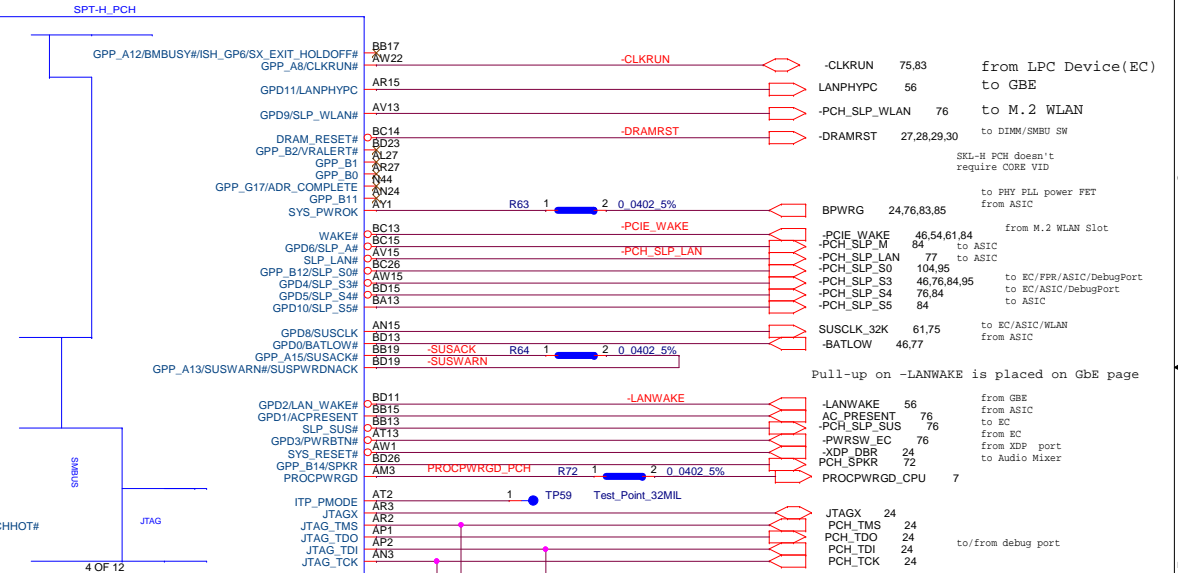
1 TP5 2
Test_Point_20MIL

1 TP6 2
Test_Point_20MIL

TEST PAD

BOTTOM SIDE

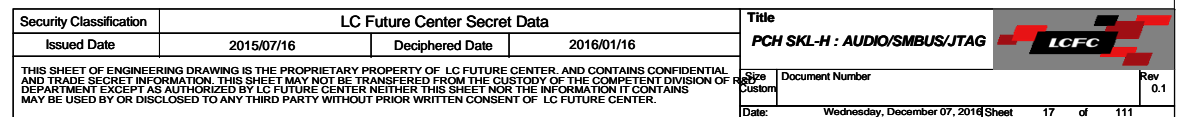
DO NOT MOVE AFTER FIX



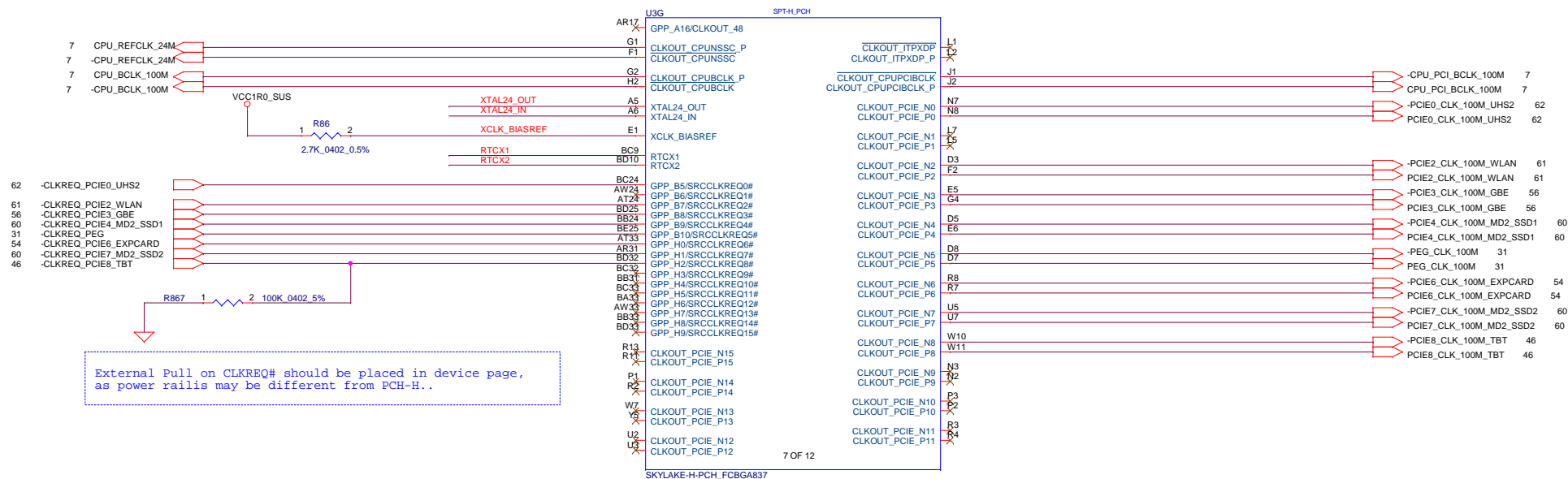
GPP_C5/SML0ALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default by internal PD)



R86 Need change to 2.71K_0.5%

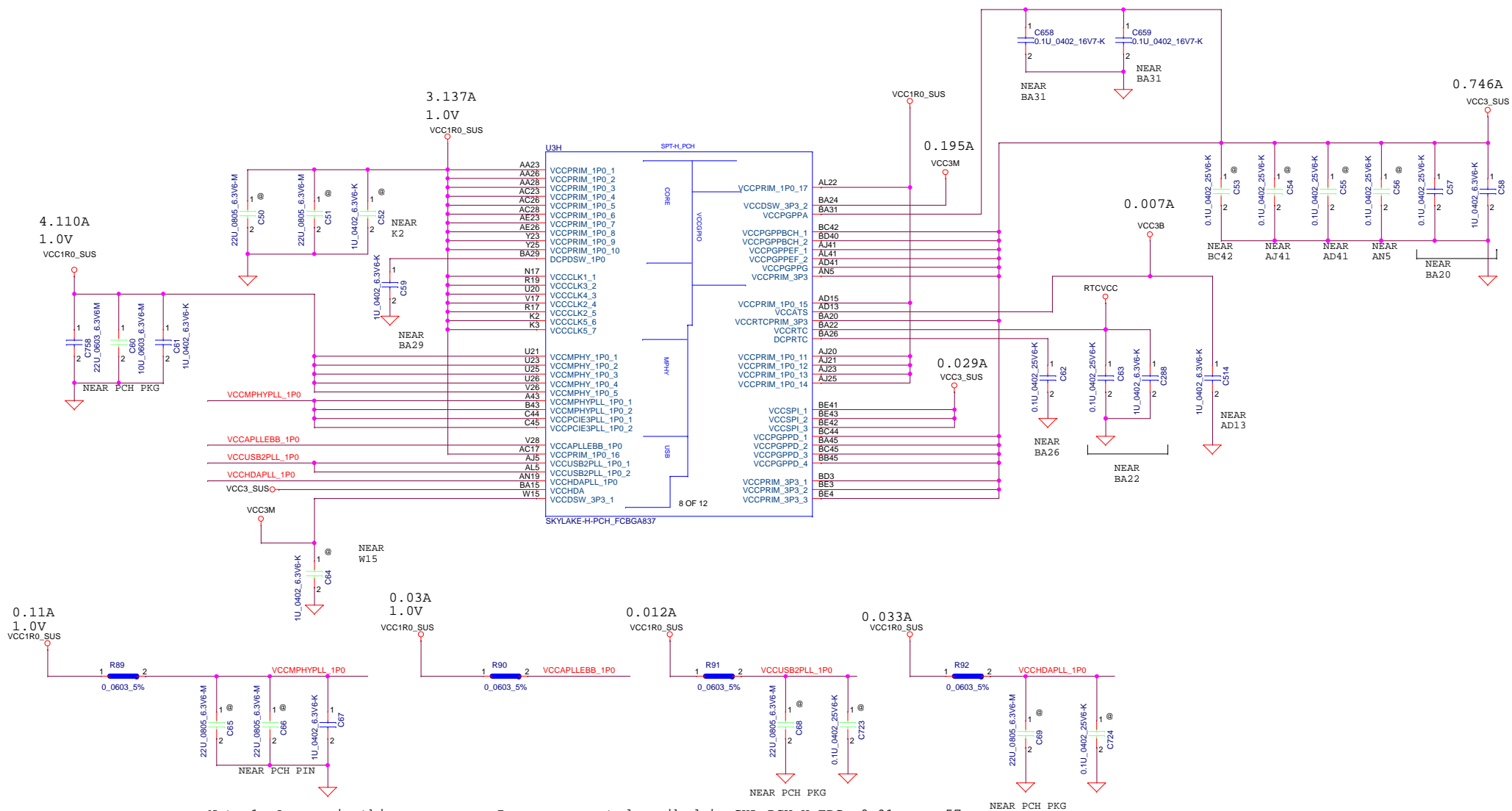


PCIE Clock Assignment

Clock 0 : UHS II
 Clock 1 : NA
 Clock 2 : Wireless LAN M.2 Slot
 Clock 3 : Giga Bit Ethernet
 Clock 4 : PCIe SSD on M.2 Slot
 Clock 5 : Discrete GFX(MXM or Onboard)
 Clock 6 : Express Slot
 Clock 7 : PCIe SSD on M.2 Slot
 Clock 8 : Thunderbolt
 Clock 9 - 15 : NA


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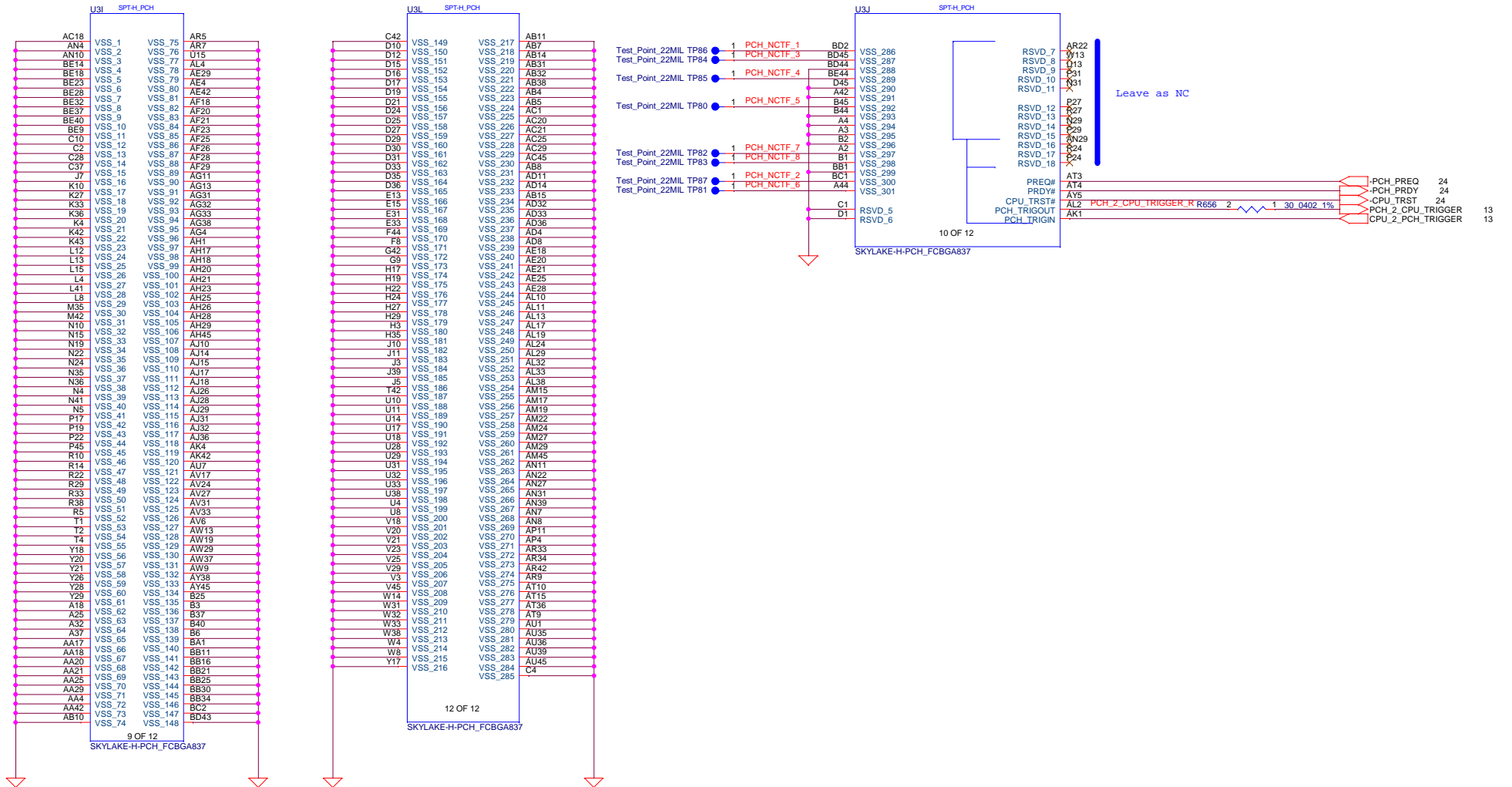
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PCH SKL-H : CLK		Rev 0.1	
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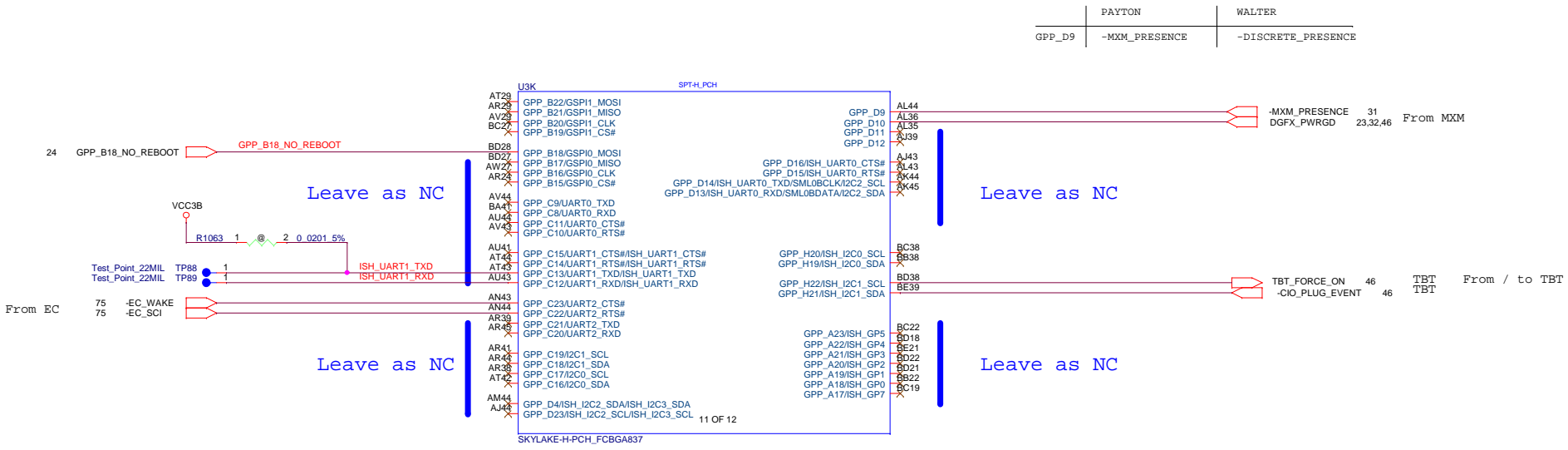


Note 1: Ampere in this page means Iccmax current described in SKL PCH H EDS r0.91 page 57.

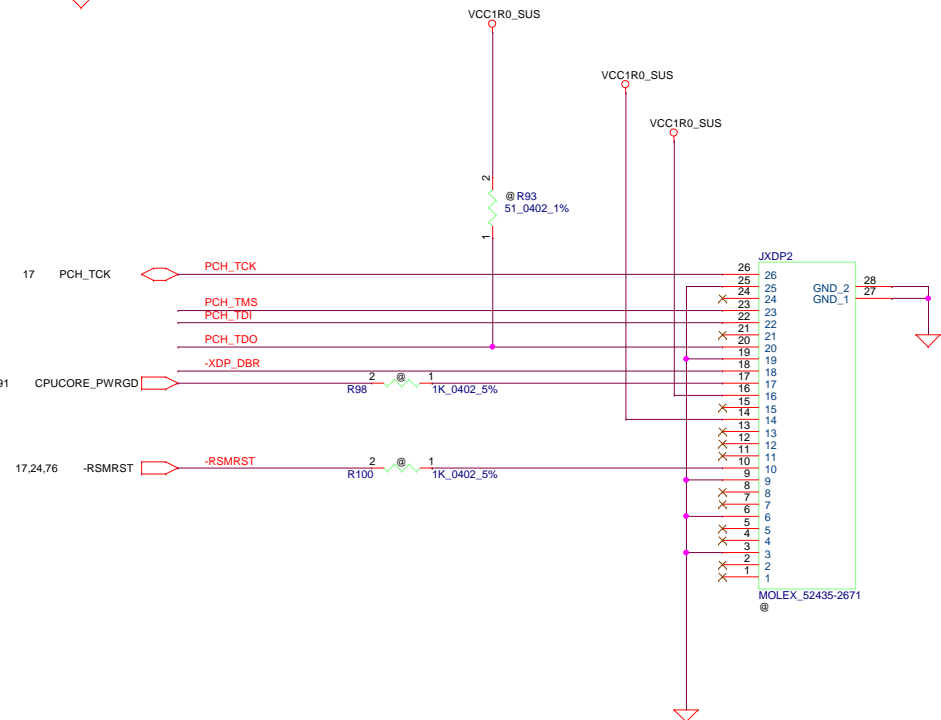
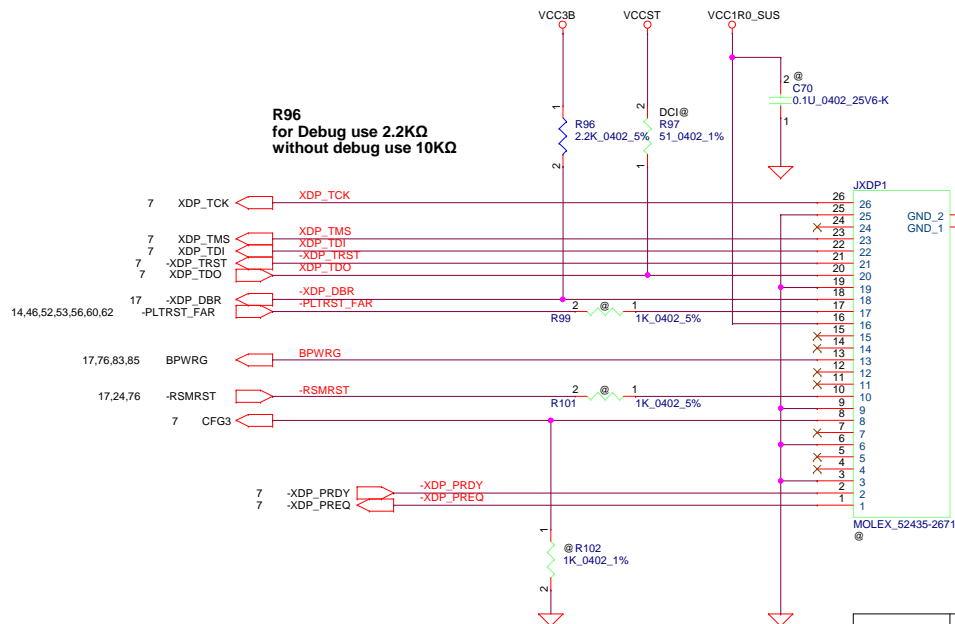
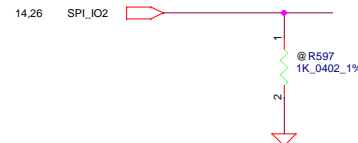
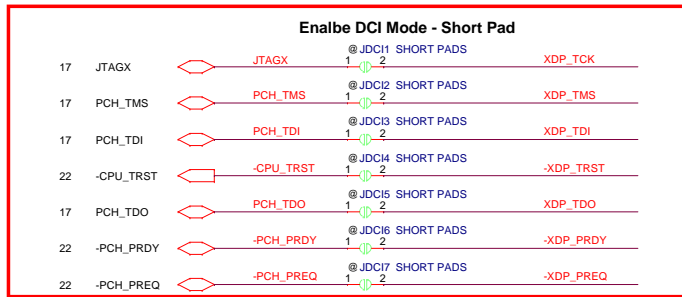
Note 2: Decoupling capacitors refers SKL H PDG r0.71 page 526.
SKL H RVP11 schematics r0.7 also referred.

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	PAYTON	WALTER
GPP_D9	-MXM_PRESENCE	-DISCRETE_PRESENCE



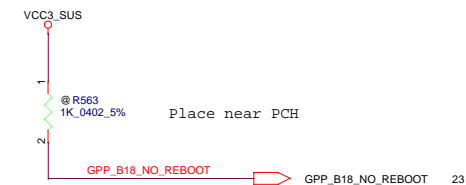
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R18	NO ASM	ASM	ASM
R297	NO ASM	ASM	NO ASM

	No use	Individual Port	DCI 2.0 w/o connector
R97	NO ASM	ASM	ASM
J1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	ASM	ASM	ASM
R101	NO ASM	ASM	NO ASM
R93	NO ASM	ASM	NO ASM
J2	NO ASM	ASM	NO ASM
R98	NO ASM	ASM	NO ASM
R100	NO ASM	ASM	NO ASM

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

← LOGIC



SHEET 7

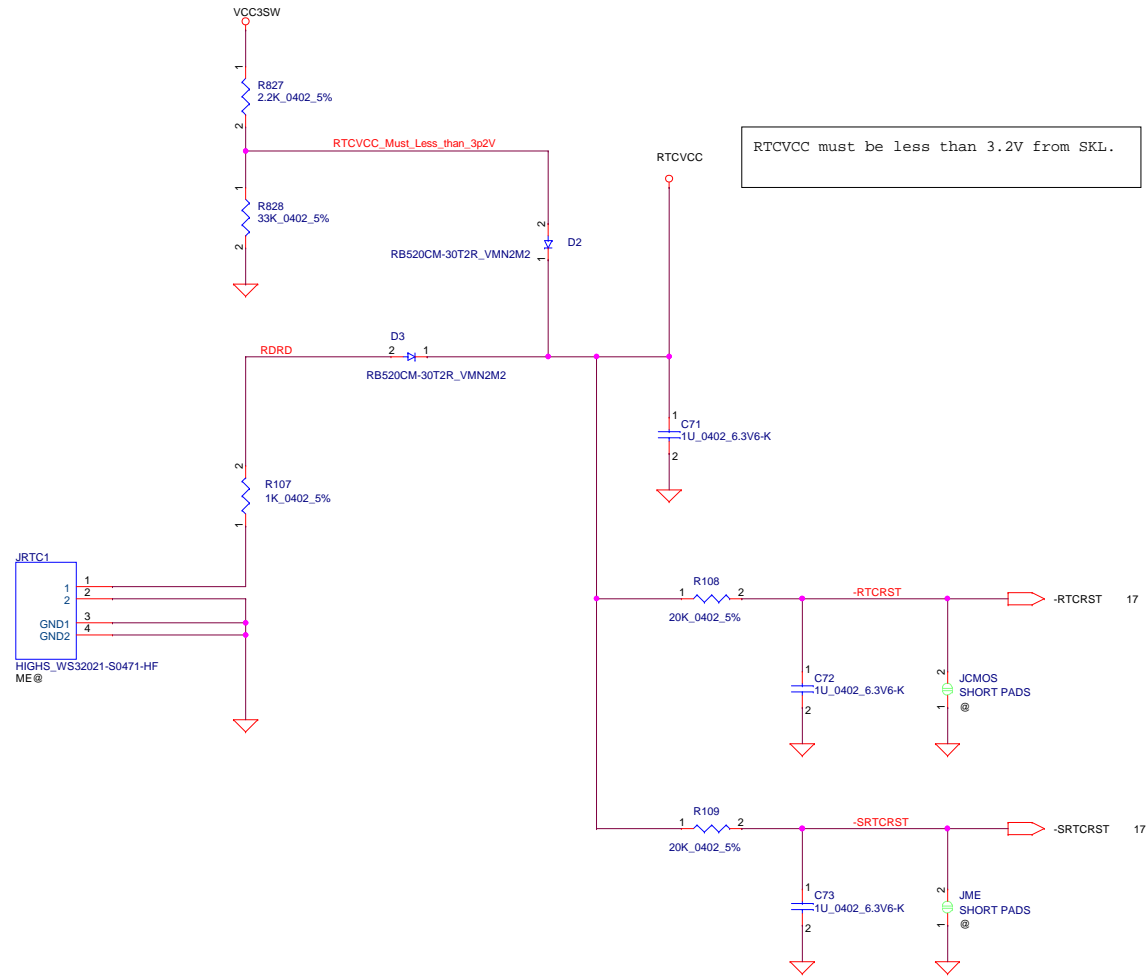
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R820	NO ASM	ASM	NO ASM
R821	NO ASM	ASM	NO ASM
R822	NO ASM	ASM	NO ASM

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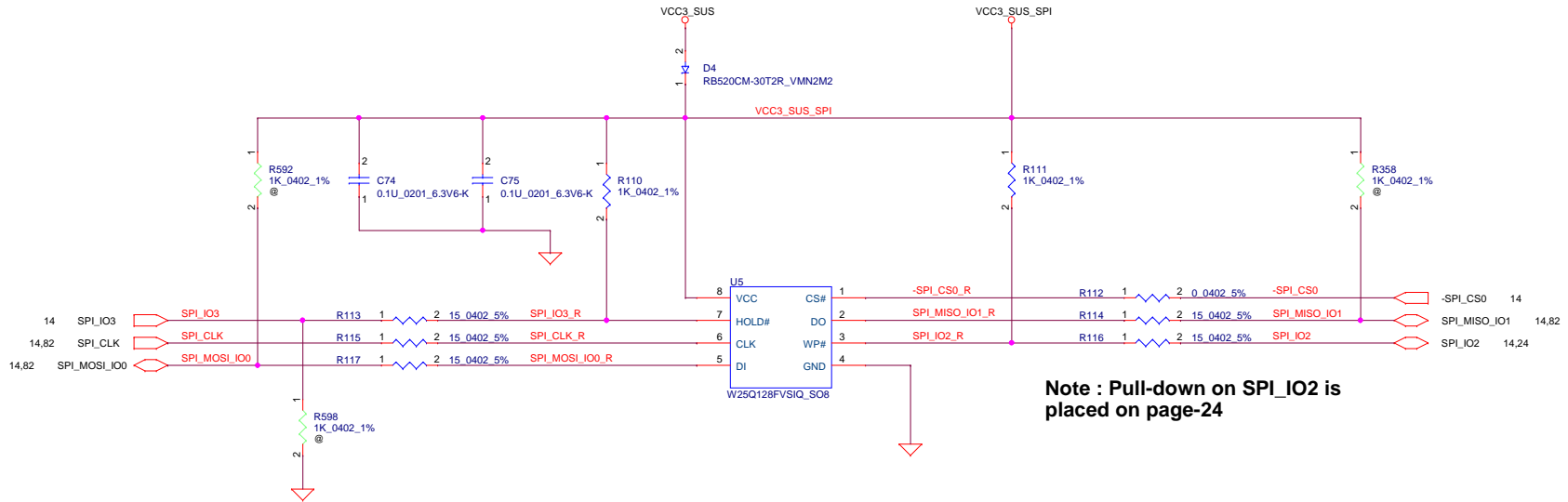
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Custom	PAYTON		
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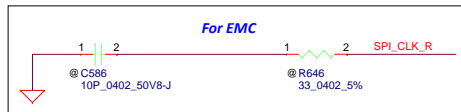
	R110	R598	U5	R592	R358
PRE ES1 ES1/ ES2	NO ASM	ASM	QE="1"	ASM	ASM
AFTER QS	ASM	NO ASM	QE=Don't Care	NO ASM	NO ASM

← LOGIC



TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R681.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		



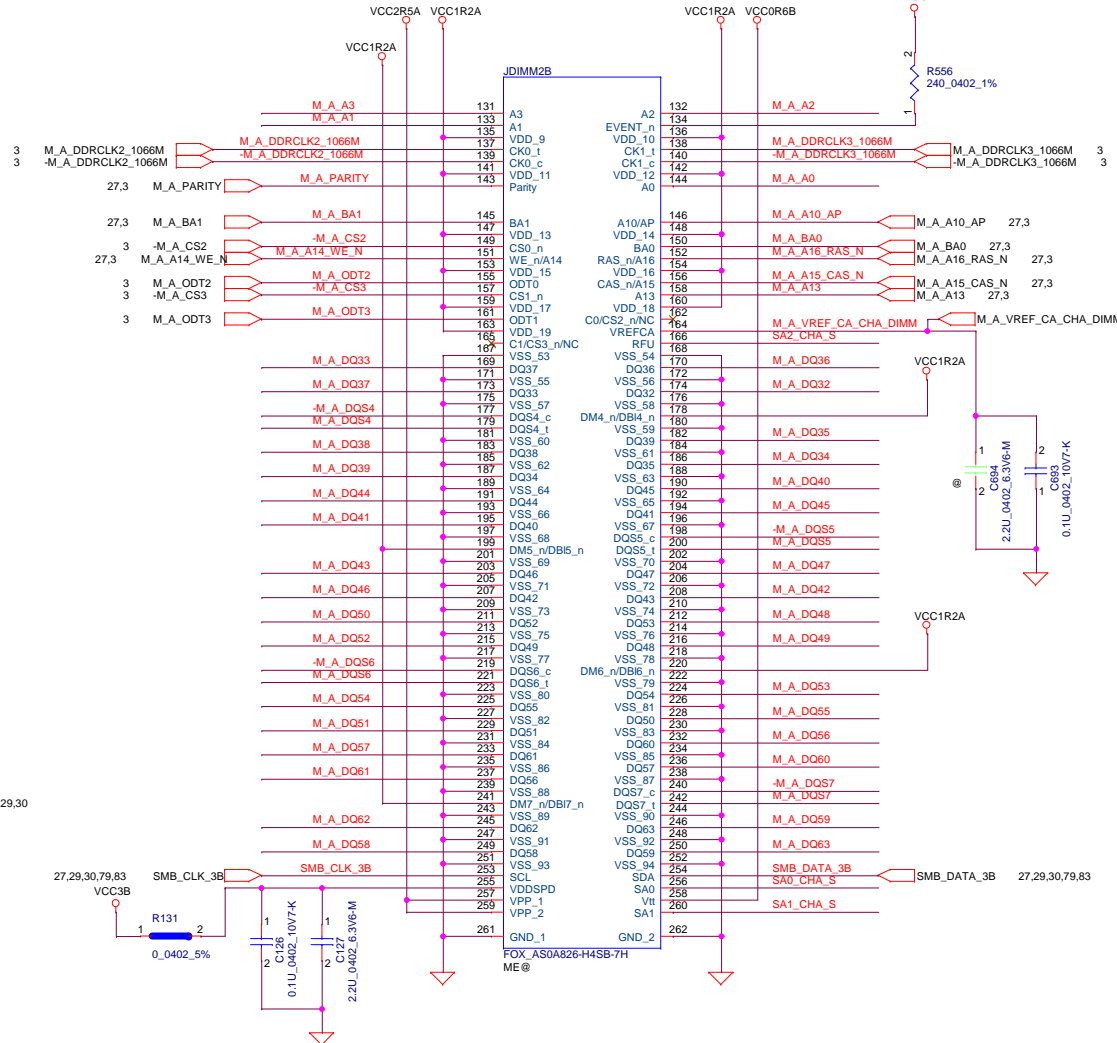
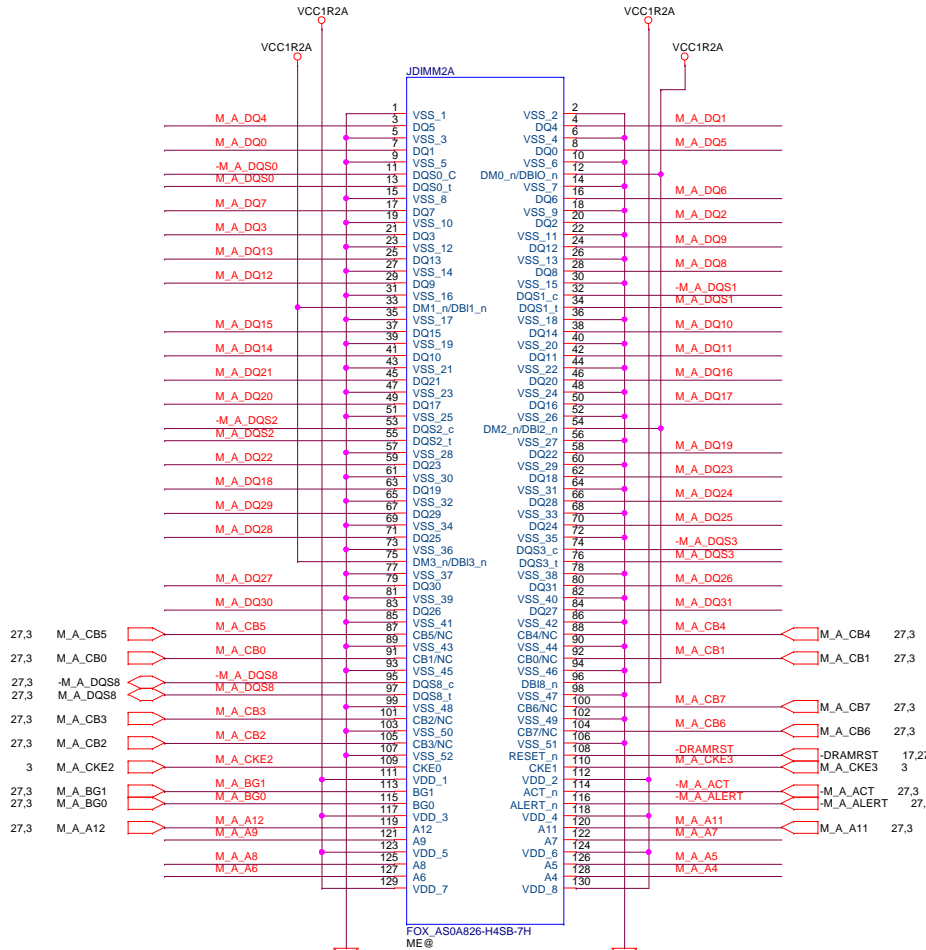
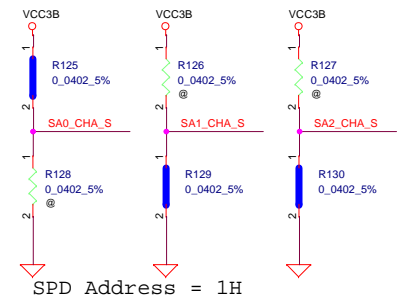
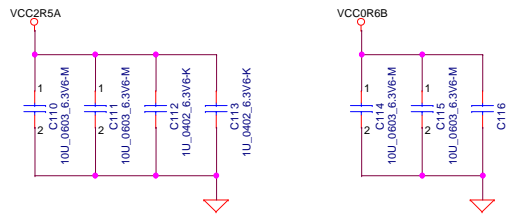
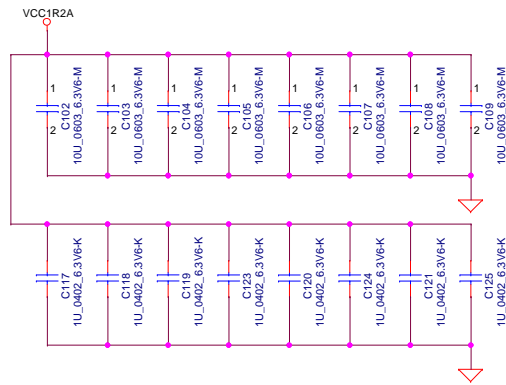
U5 SPI ROM


vPRO model(16MB)	
WINBOND	W25Q128FVSIQ
MACRONIX	MX25L12873FM2L-10G
MICRON	N25Q128A13ESEDFF

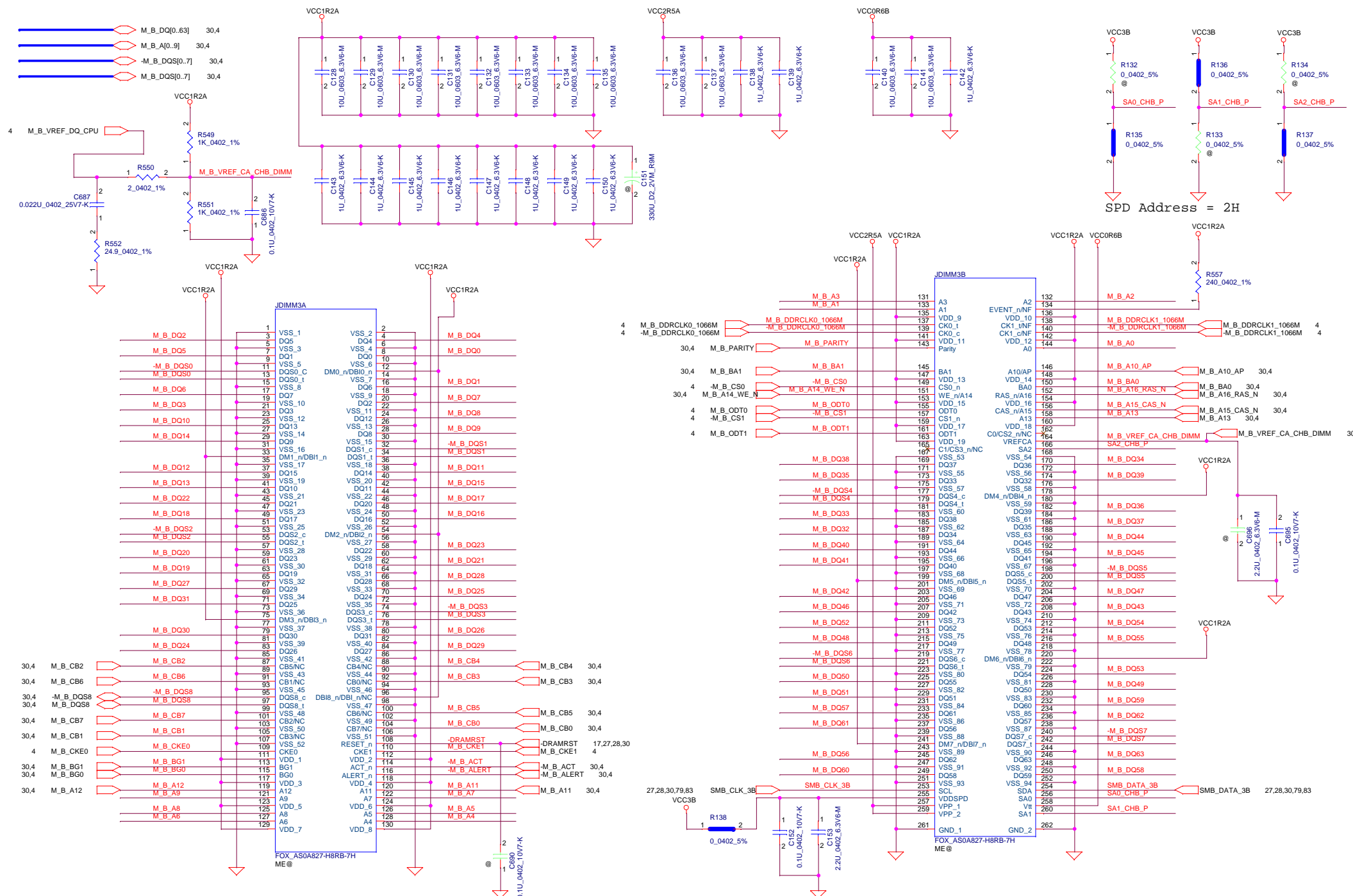
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Issued Date	2015/07/16	Deciphered Date
		2016/01/16
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Title		LCFC	
SPI FLASH			
Size	Document Number	Rev	0.1
Custom			
Date:	Wednesday, December 07, 2016	Sheet	26 of 111

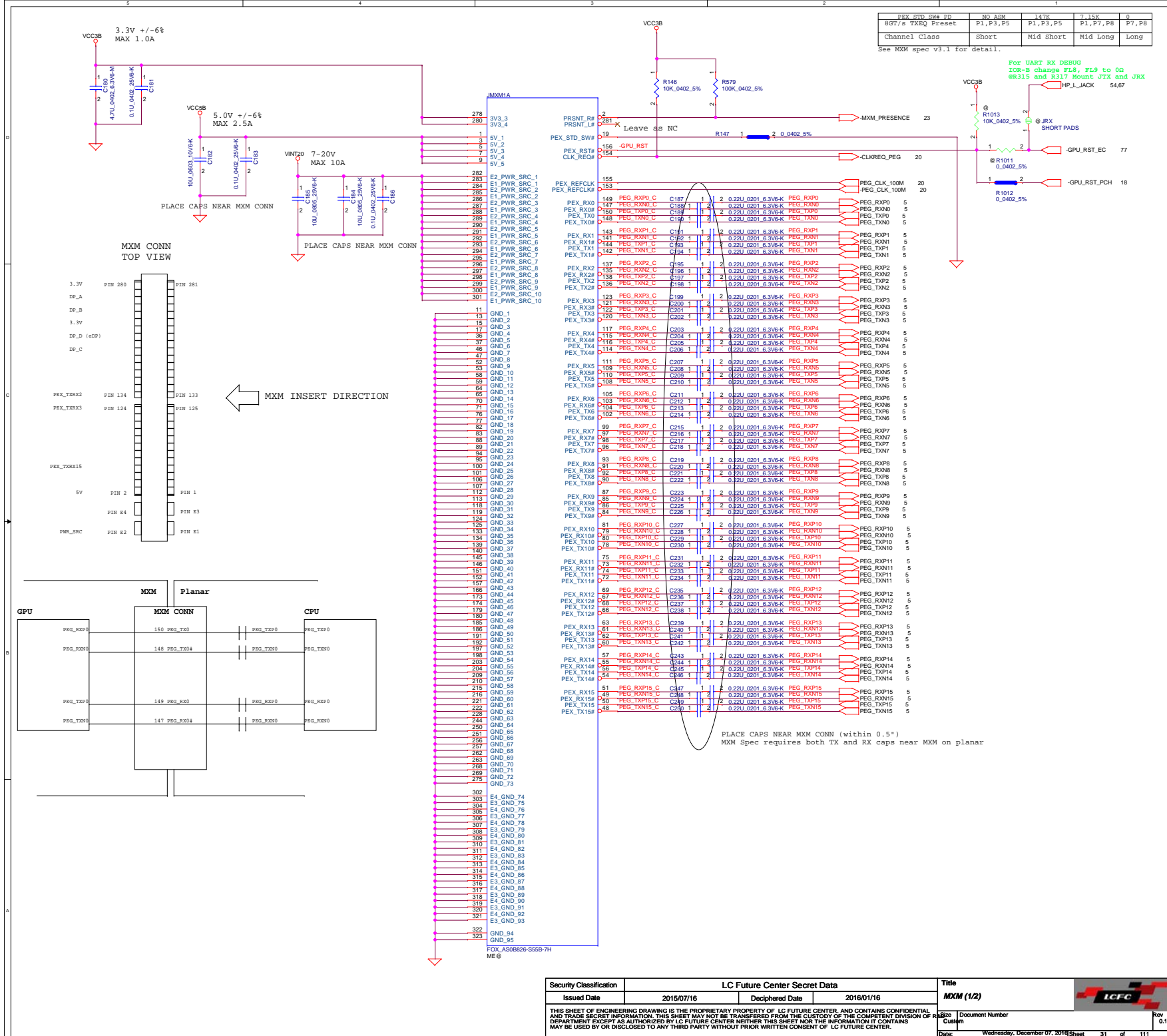
M_A_DQ[0..63] 27.3
M_A_A[0..9] 27.3
-M_A_DQS[0..7] 27.3
M_A_DQS[0..7] 27.3



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Issued Date	2015/07/16	Deciphered Date	2016/01/16	DDR4 CH-A SECONDARY		
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				Custom		0.1
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SPD Address = 2H



PEX STD SW#	PD	NO ASM	147K	7.15K	0
8Gt/s TXEQ Preset	P1,P3,P5	P1,P3,P5	P1,P7,P8	P7,P8	
Channel Class	Short	Mid Short	Mid Long	Long	

See MXM spec v3.1 for detail.

For UART RX DEBUG
IOR-B change FL8, FL9 to 00
0R315 and R317 Mount JTX and JRX

PLACE CAPS NEAR MXM CONN (within 0.5")
MXM Spec requires both TX and RX caps near MXM on planar

PU on DGFX_PWRGD is VCC3_SUS to avoid floating on PCH.

Panel ctrl signals have 100k pull-down on MXM.

To read GPU temperature by EC

-VIDEO_THERM_OVERT: LOW = Critical high temp detected on MXM. Need to shutdown in 500 ms. From MXM to EC(?). Open Drain, 100k on both planar and MXM.
-VIDEO_THERM_ALERT: HIGH = full power, LOW = reduced power. Used for thermal management. From EC to MXM. Open Drain, 100k on both planar and MXM.


MXM_ON: HIGH = To power on MXM. From EC to MXM. Push-pull.

-VIDEO_POWER_LIMIT: HIGH = full power, LOW = reduced power. From EC to MXM. Open Drain, 100k PU to VCC3B on MXM.


MXM OEM / GPIO PIN3	N16E-Q1/-Q3/-Q5		N16M-Q2	
	Signal Name	I/O Tpye	Signal Name	I/O Tpye
OEM4	GPU_EVENT#	Bi-Dir	GPU_EVENT#	Bi-Dir
OEM5	GC6_FB_EN	IN	GC6_FB_EN	IN
OEM6	GPIO19_STEREO	OUT	GPIO7_STEREO	OUT
OEM7	FRAMELOCK	IN	FRAMELOCK#	IN
GPIO0	GPIO26	Tri-state	NC(Default)	NC
GPIO1	GPIO25	Tri-state	NC(Default)	NC
GPIO2	GPIO25	Tri-state	NC(Default)	NC

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	MXM (2/2)	
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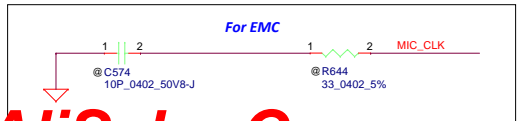
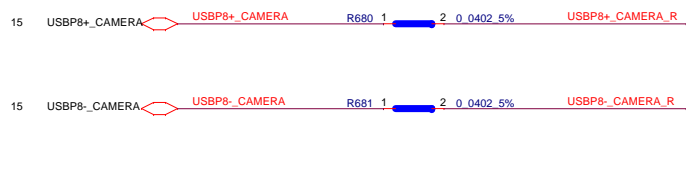
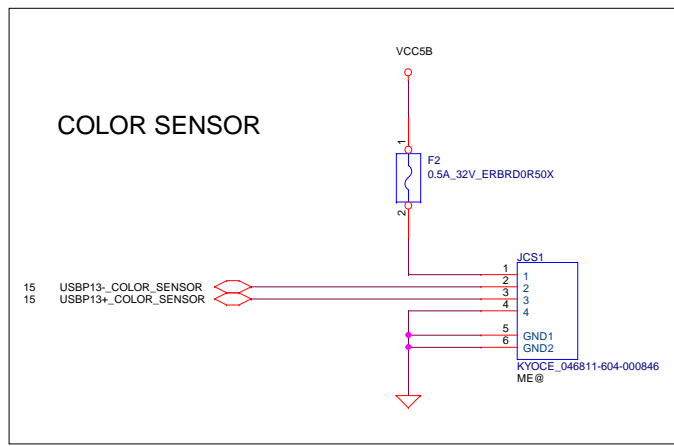
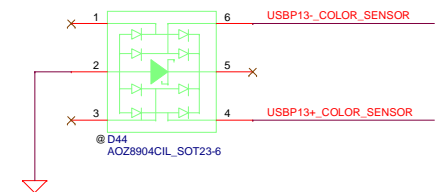
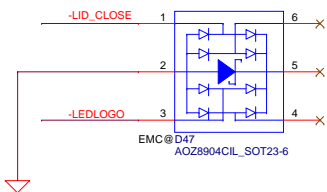
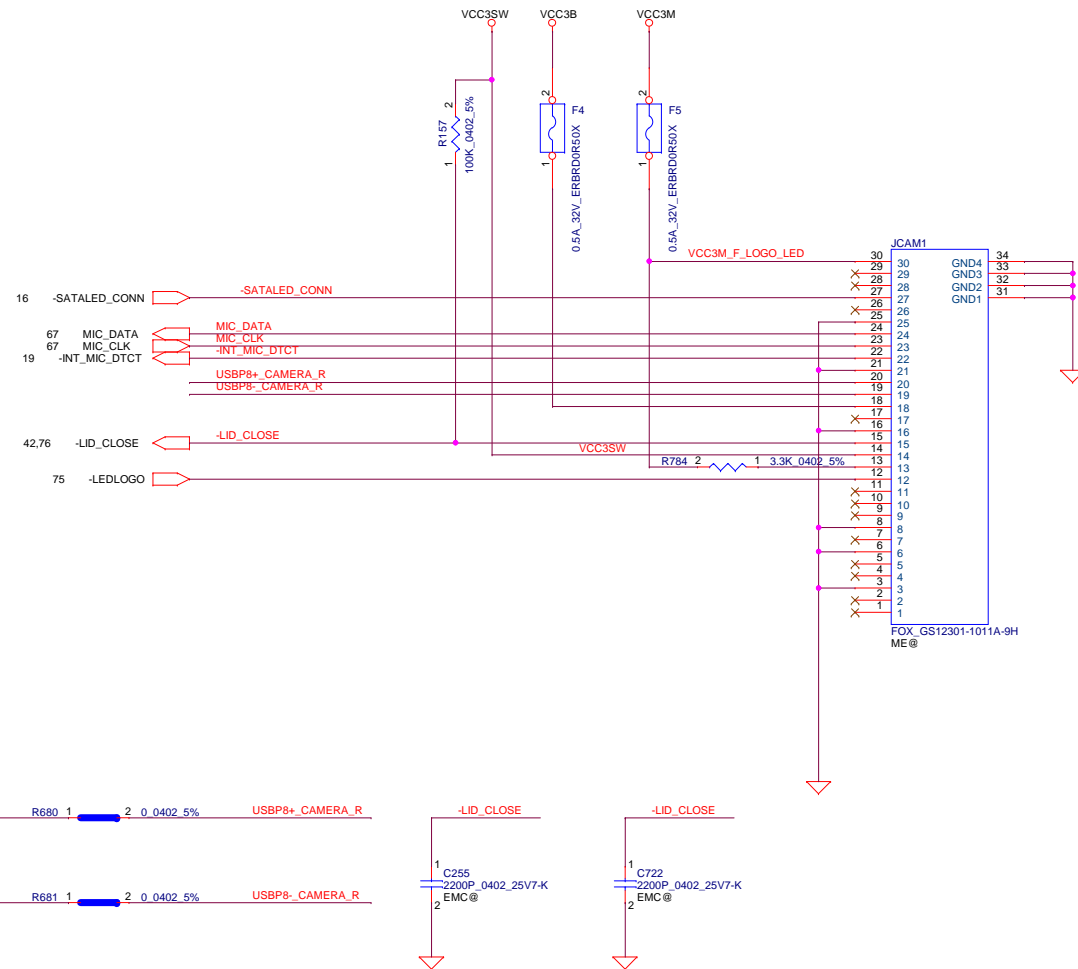
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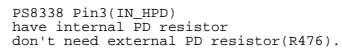
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INDICATOR LED
2D CAM/MIC/(LID)
LOGO LED/LID

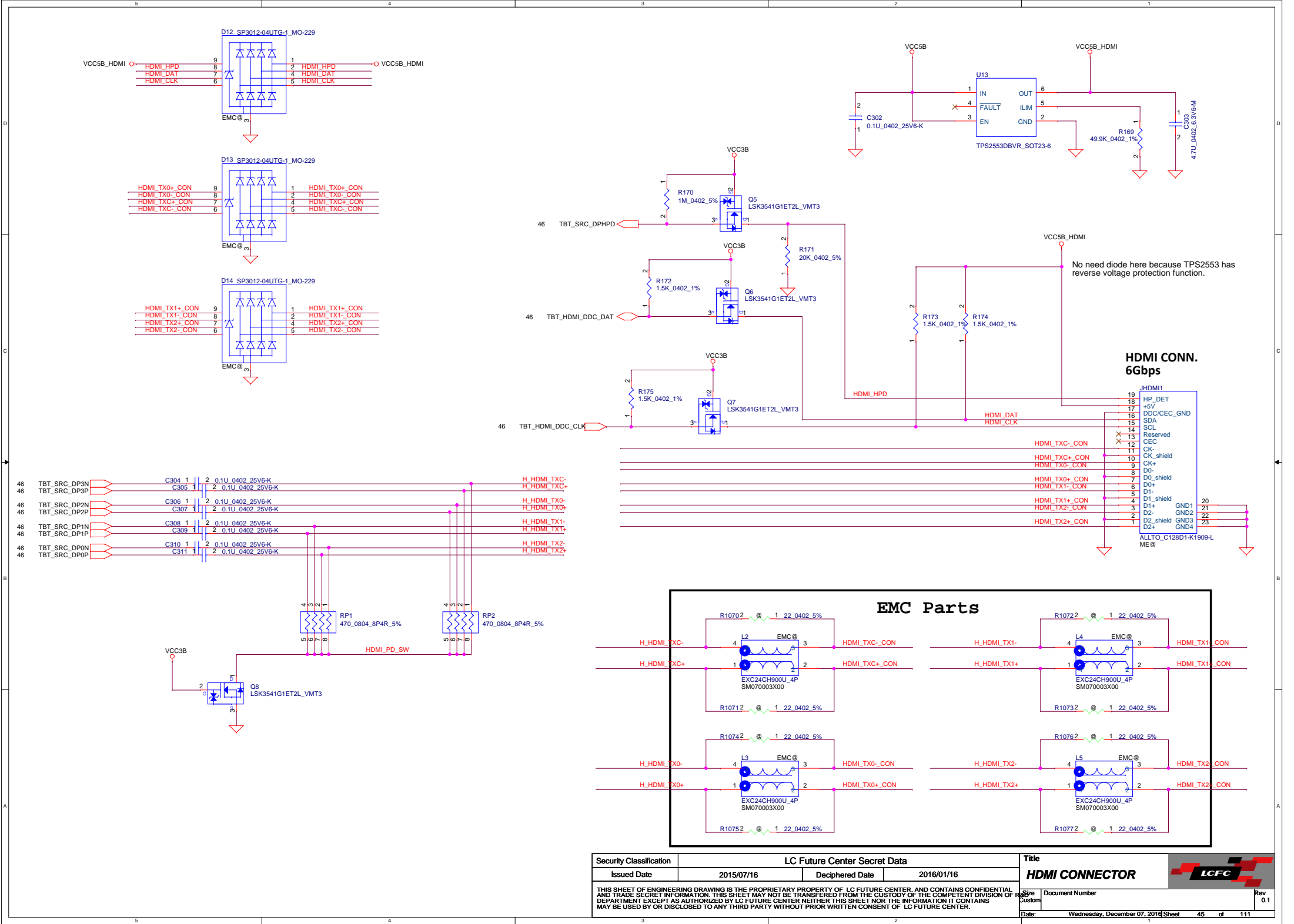


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DP_DGL_DTCT	DP MODE	2SK3541	RTM002	AUXP/N
LOW	DP (Native)	OFF	OFF	No pull-up
HIGH	TMDS (Dongle)	ON	ON	Pull up to 4.7k




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Issued Date	2015/07/16	Deciphered Date	2016/01/16	DISPLAY PORT CONNECTOR					
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Issued Date		2015/07/16	Deciphered Date	2016/01/16	HDMI CONNECTOR		
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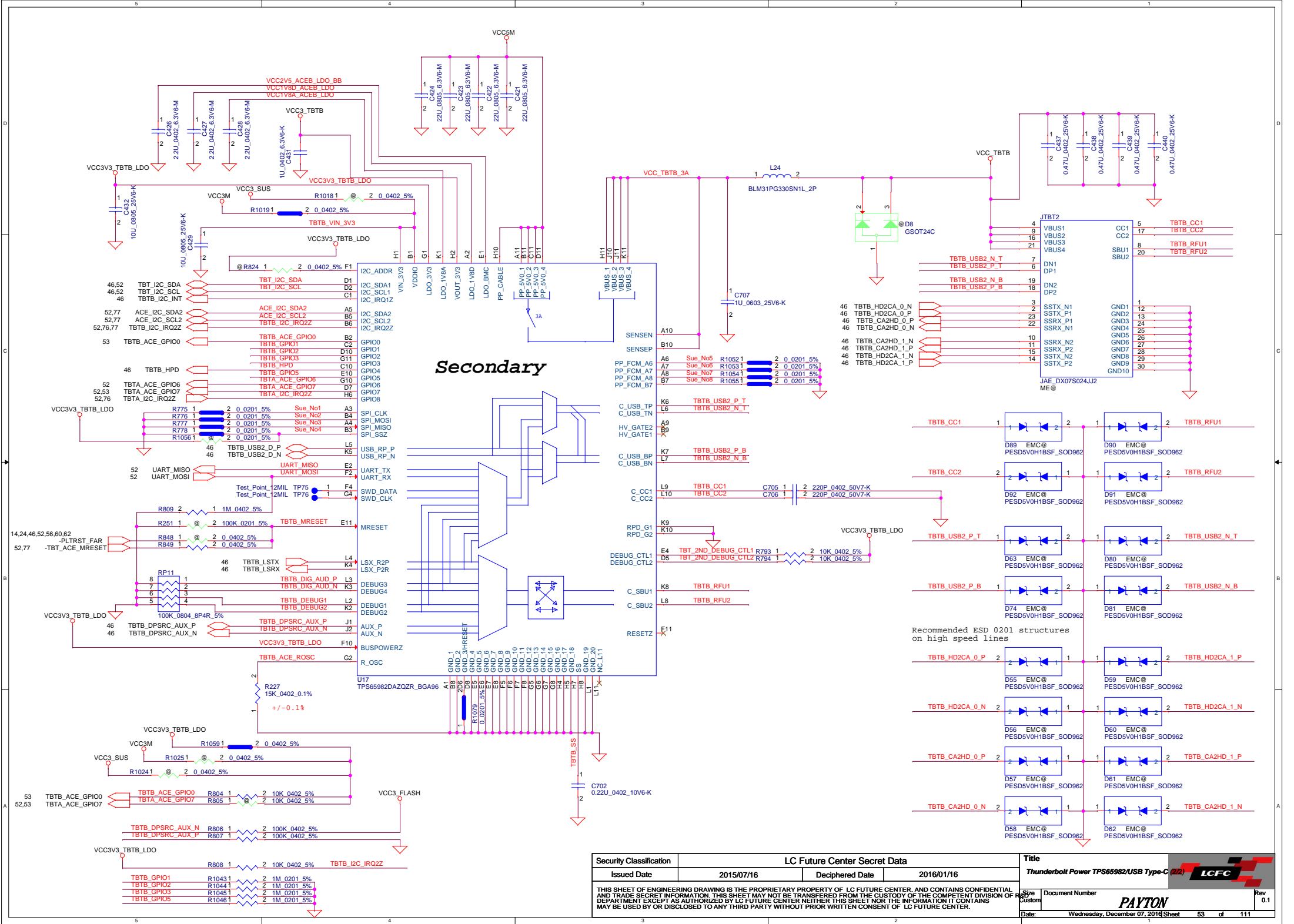
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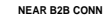
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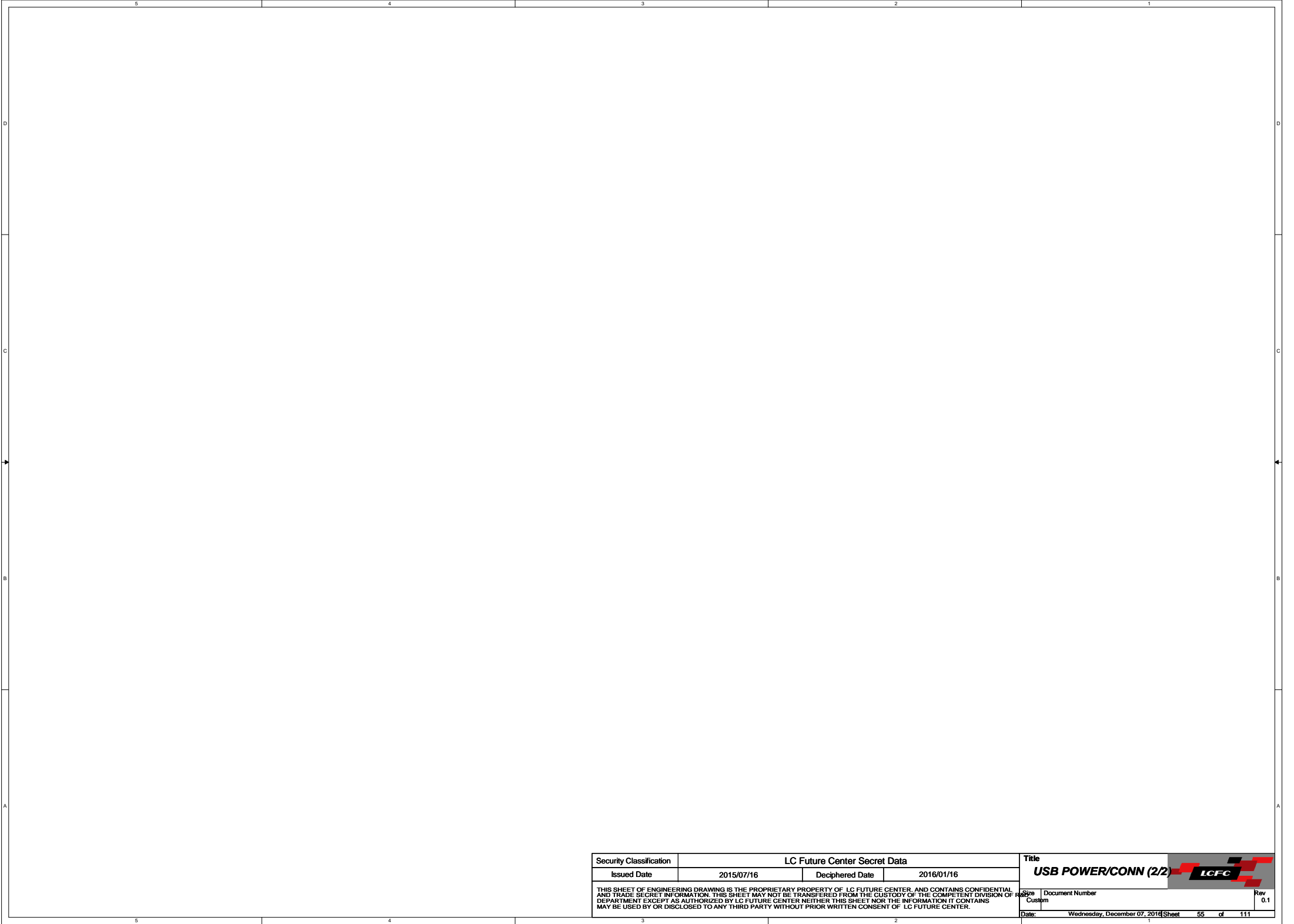
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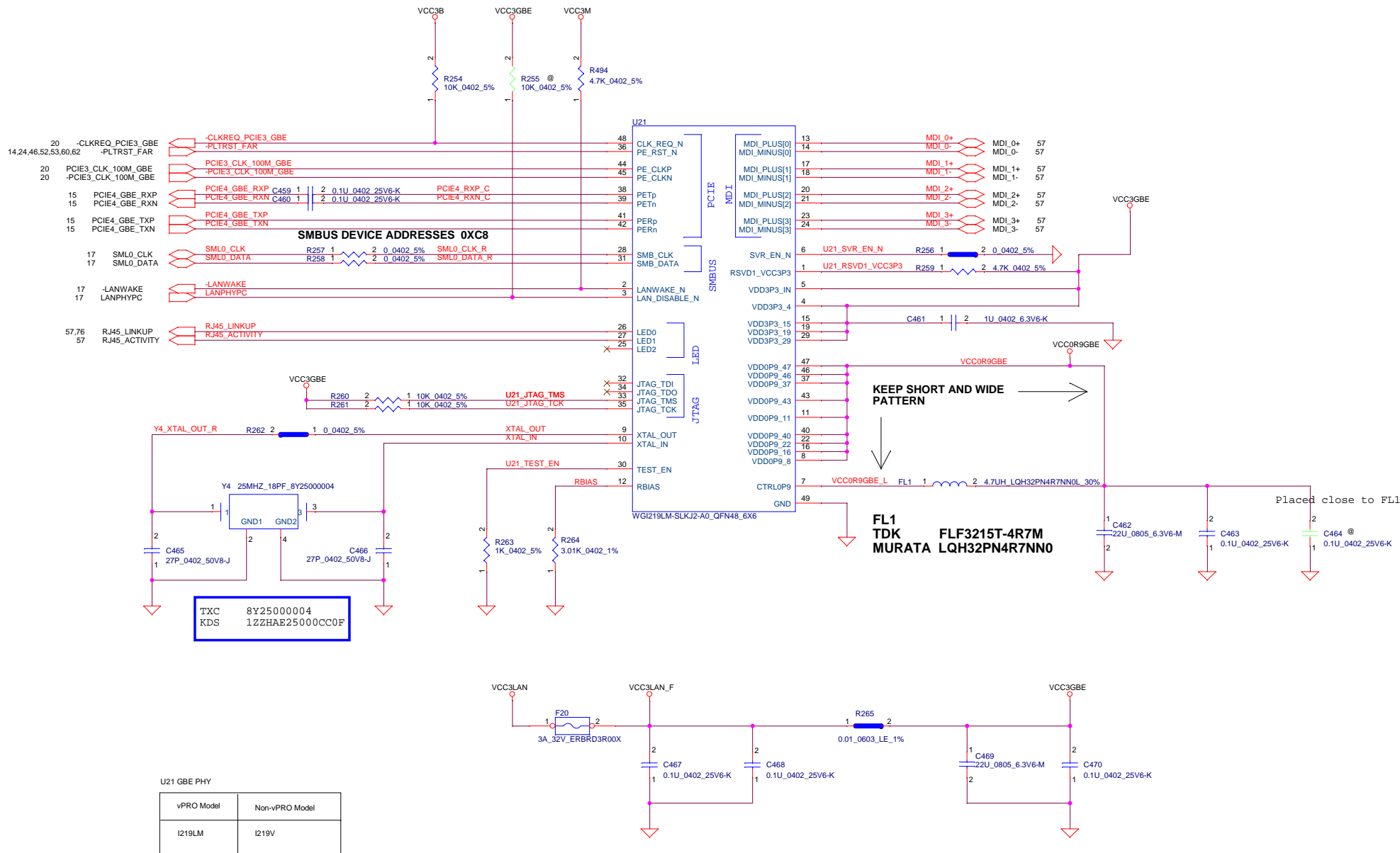


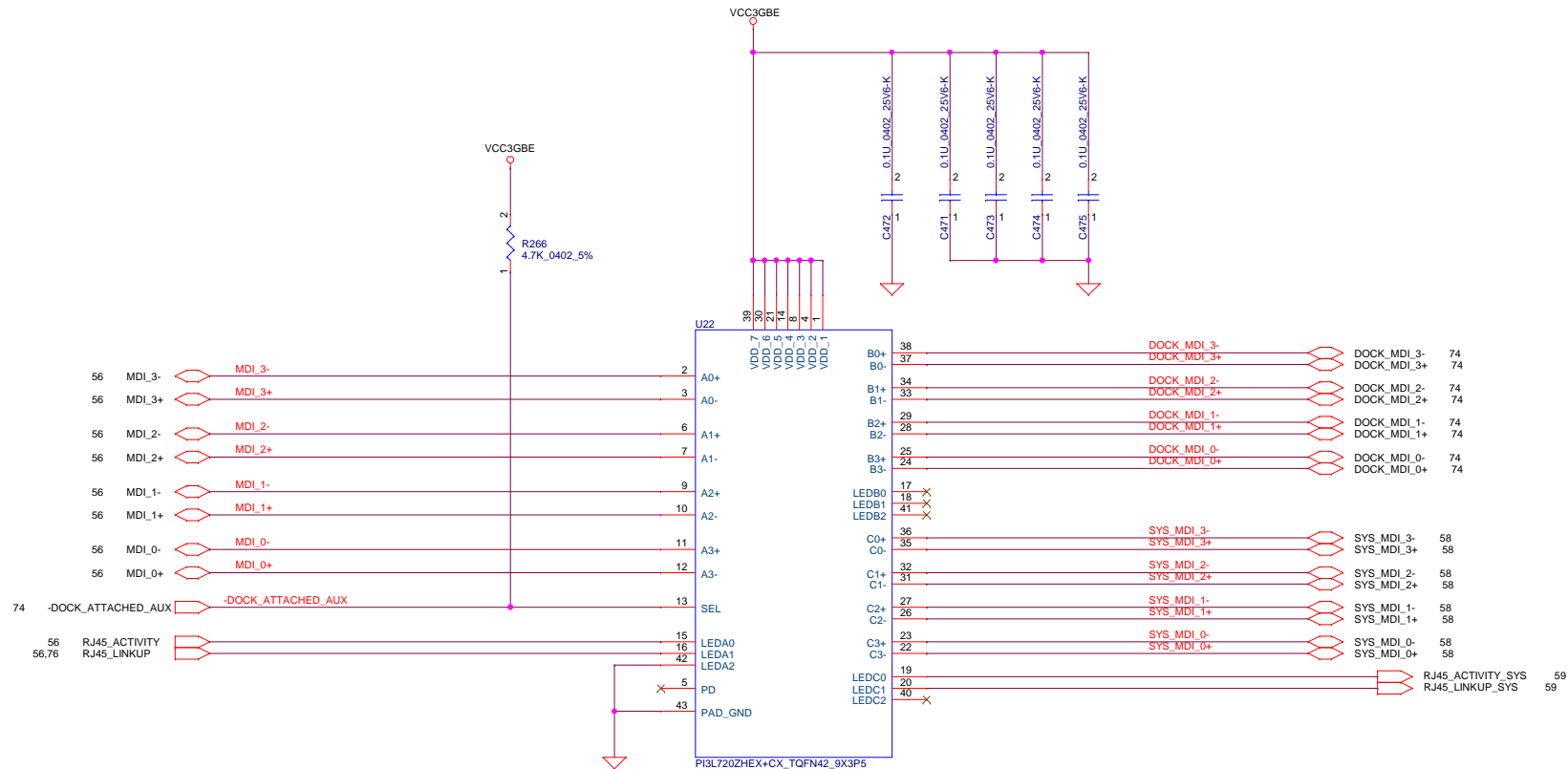




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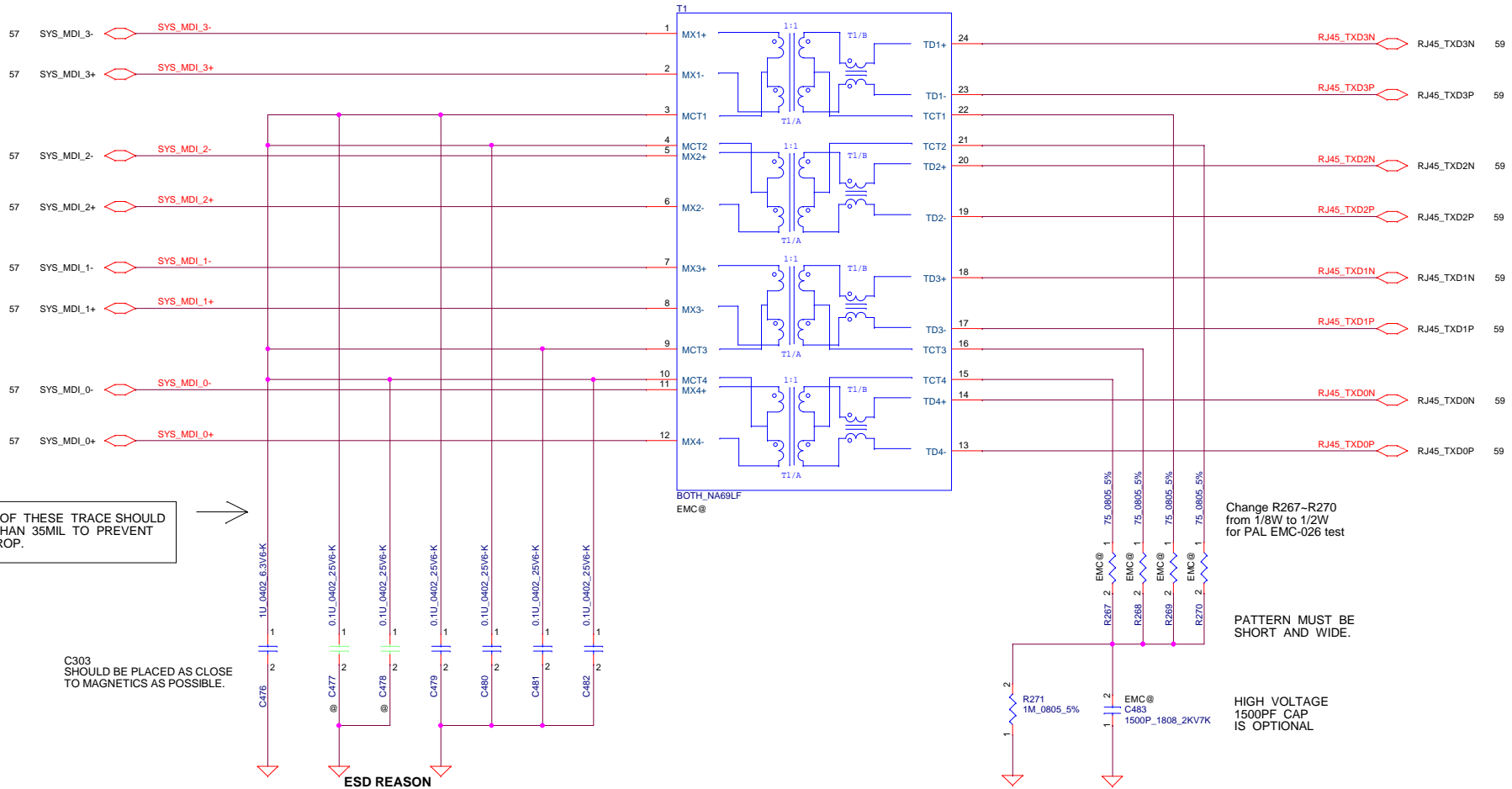
Vendor	P/N
Pericom TI	PI3L720ZHEX+CX TS3L501E

Security Classification	LC Future Center Secret Data			
Issued Date	2015/07/16	Deciphered Date	2016/01/16	
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GBE LAN SWITCH		Custom		Wednesday, December 07, 2016	
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PAYTON



THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

ESD REASON

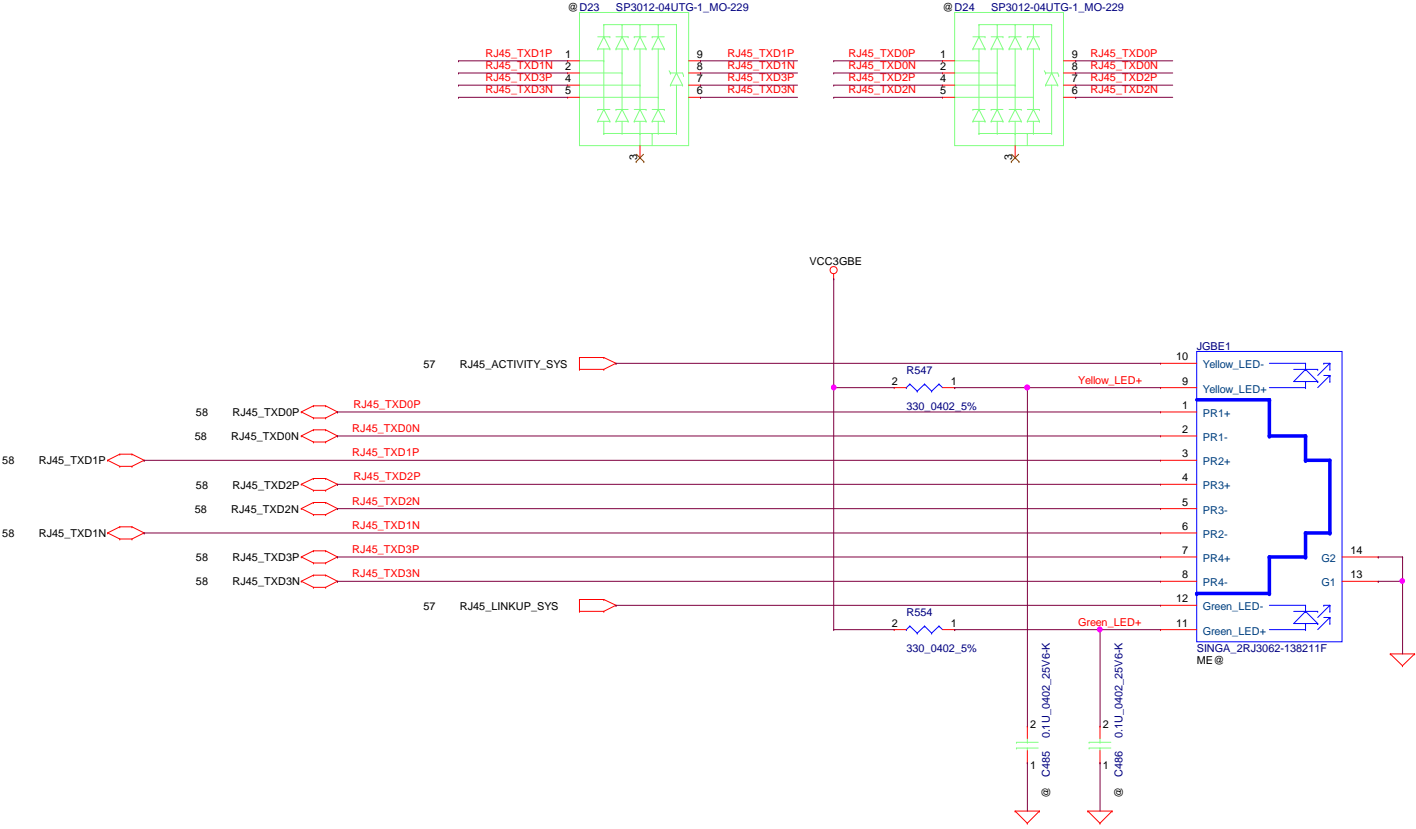
Change R267-R270 from 1/8W to 1/2W for PAL EMC-026 test

PATTERN MUST BE SHORT AND WIDE.

HIGH VOLTAGE 1500PF CAP IS OPTIONAL

Vendor	P/N
Timag	IH-115-F
Bothhand	NA69LF

D23, D24 EMC Parts



PCH	Planar	Socket	M.2 PCIe SSD Module	Chip
PCIE9_RXP/SATA0A_RXP	PCIE9L0_SATA0A_MD2_SSD1_RXP	41: PERM0/SATA_B+	41: PETN0	
PCIE9_RXN/SATA0A_RXN	PCIE9L0_SATA0A_MD2_SSD1_RXN	43: PERP0/SATA_B-	43: PETP0	
PCIE9_TXN/SATA0A_TXN	PCIE9L0_SATA0A_MD2_SSD1_TXN	47: PETN0/SATA_A-	47: PERN0	
PCIE9_TXP/SATA0A_TXP	PCIE9L0_SATA0A_MD2_SSD1_TXP	49: PETP0/SATA_A+	49: PERP0	

PCH	Planar	Socket	M.2 SATA SSD Module	Chip
PCIE9_RXP/SATA0A_RXP	PCIE9L0_SATA0A_MD2_SSD1_RXP	41: PERNO/SATA_B+	41: SATA B+	
PCIE9_RXN/SATA0A_RXN	PCIE9L0_SATA0A_MD2_SSD1_RXN	43: PERP0/SATA_B-	43: SATA B-	
	SATA: Straight			
PCIE9_TXN/SATA0A_TXN	PCIE9L0_SATA0A_MD2_SSD1_TXN	47: PETN0/SATA_A-	47: SATA A-	
PCIE9_TXP/SATA0A_TXP	PCIE9L0_SATA0A_MD2_SSD1_TXP	49: PETP0/SATA_A+	49: SATA A+	

[illegible]

VCC3B

R274
10K_0402_5%

PEDET_SSD1

-PCIE_DETECT_SSD1

Q13
LSK3541G1ET2L_VMT3

PEDET (PE_DTCT)
SATA Device
PCIe Device

GND
Open

-PCIE_DETECT_SSD1	Device
High	SATA SSD
Low	PCIe SSD

-PCIE_DETECT_SSD2	Device
High	SATA SSD
Low	PCIe SSD

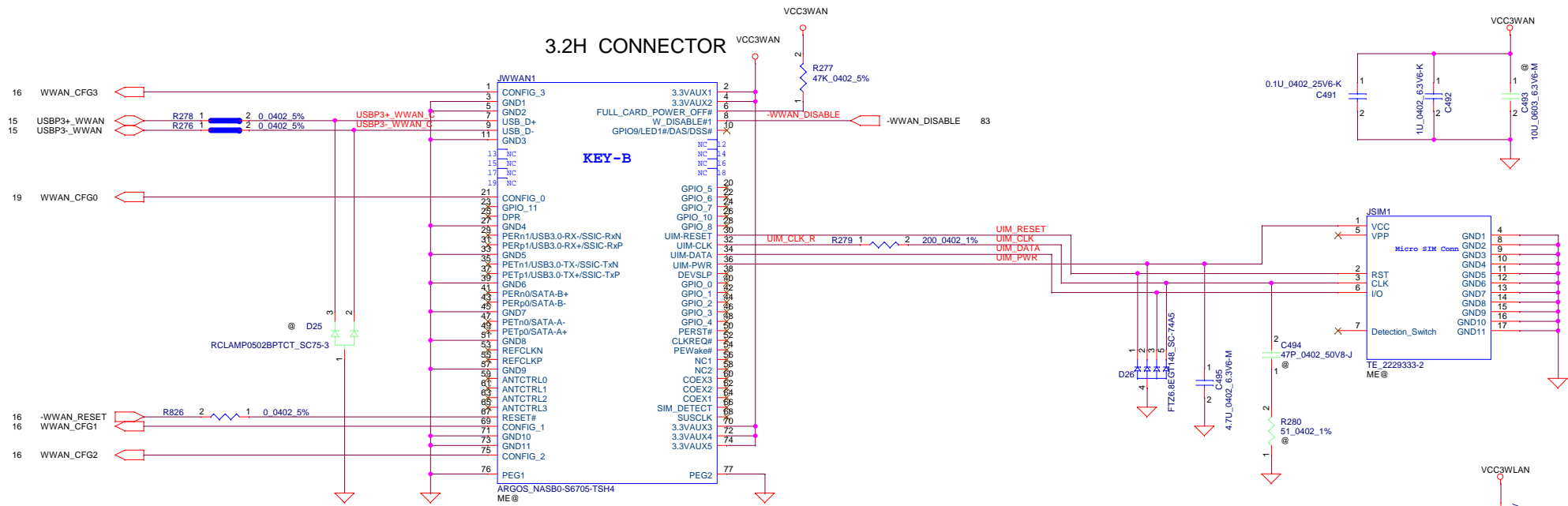
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Title			
M.2 SATA/PCIE SSD CARD SLOT			
Size Custom	Document Number	Rev 0.1	
Date:	Wednesday, December 07, 2016	Sheet 60 of 111	

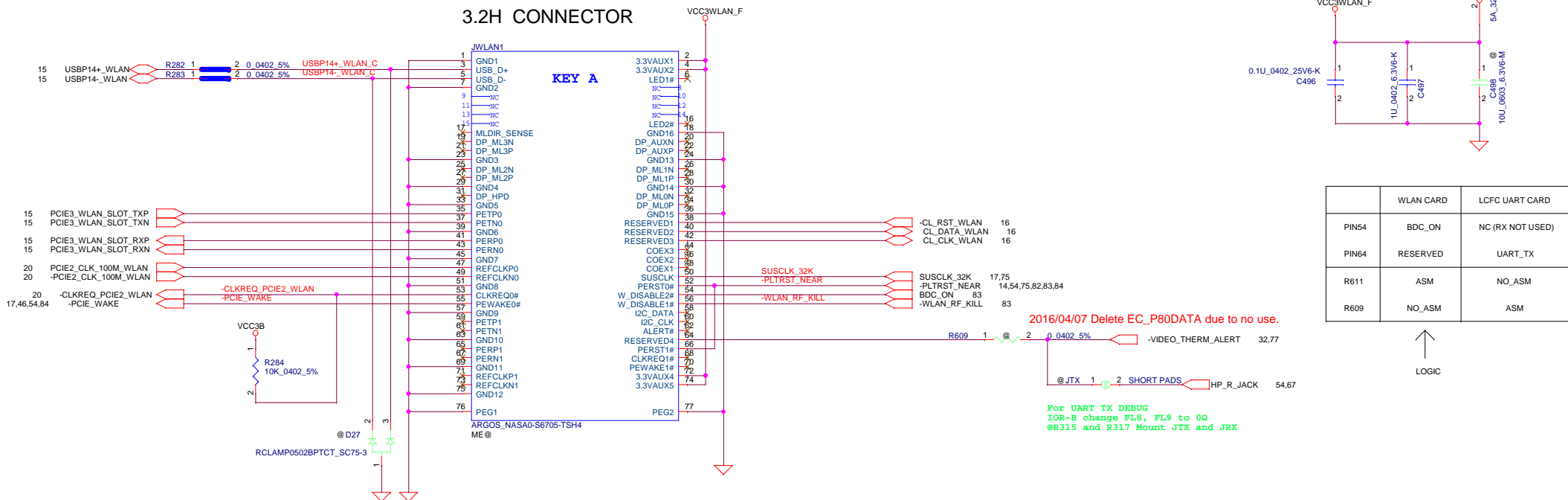
PRTC3
BATT CR2032 3V 225MAH
RTC@

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/11/08	Deciphered Date	2013/11/08	Load BOM Only(RTC BATT CR2032 3V 225MAH) LCFC	
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				Date:	Wednesday, December 07, 2016
				Sheet	60 of 60
				Rev	0.2

TYPE-B NGFF CCARD FOR WWAN



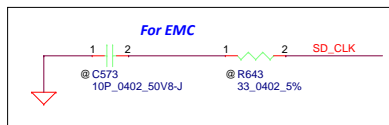
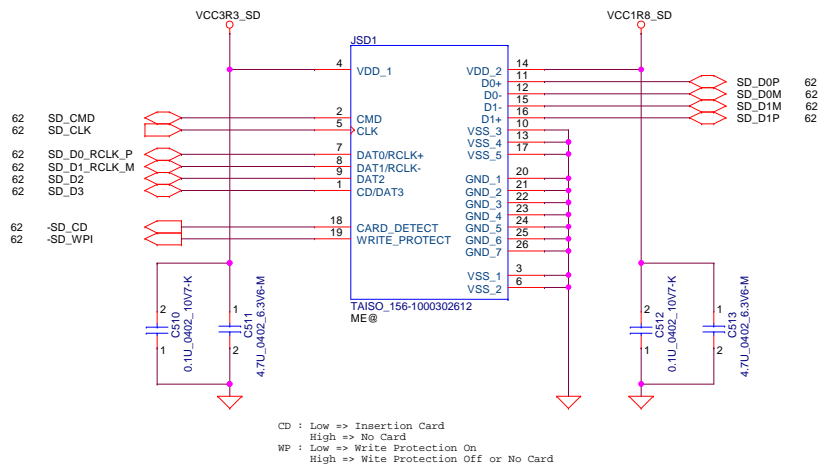
TYPE-A NGFF CCARD FOR WLAN



	WLAN CARD	LCFC UART CARD
PIN54	BDC_ON	NC (RX NOT USED)
PIN64	RESERVED	UART_TX
R611	ASM	NO_ASM
R609	NO_ASM	ASM

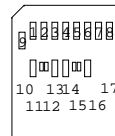
↑
LOGIC

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	M.2 WIRELESS CARD SLOT	
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				Document Number	
				PAYTON	
				Date: Wednesday, December 07, 2016	
				Sheet 61 of 111	

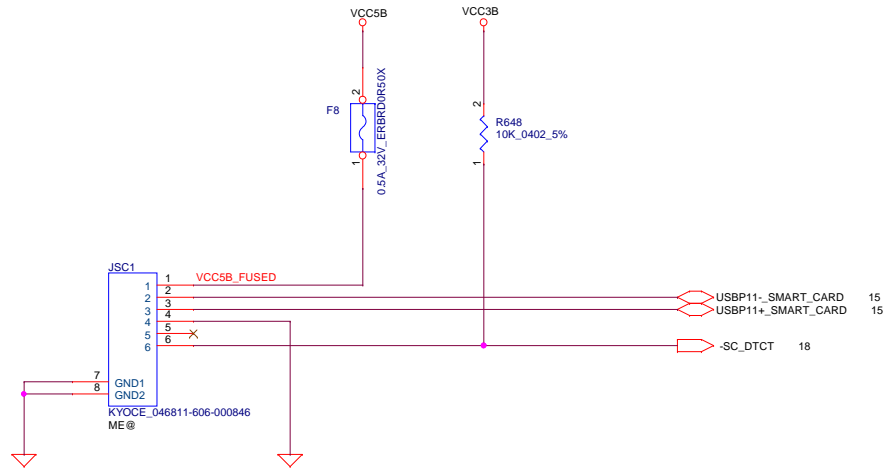



Normal type	UHS-II SD Slot	UHS II Mode
Pin No	SD Mode	
1	CD/DAT3	
2	CMD	
3	VSS1	
4	VDD	VDD1
5	CLK	
6	VSS2	
7	DAT0	RCLKP
8	DAT1	RCLKM
9	DAT2	
10		VSS3
11		D0P
12		D0M
13		VSS4
14		VDD2
15		D1M
16		D1P
17		VSS5
CD		
WP		
	CARD DETECT	
	WRITE PROTECT	

Bottom View

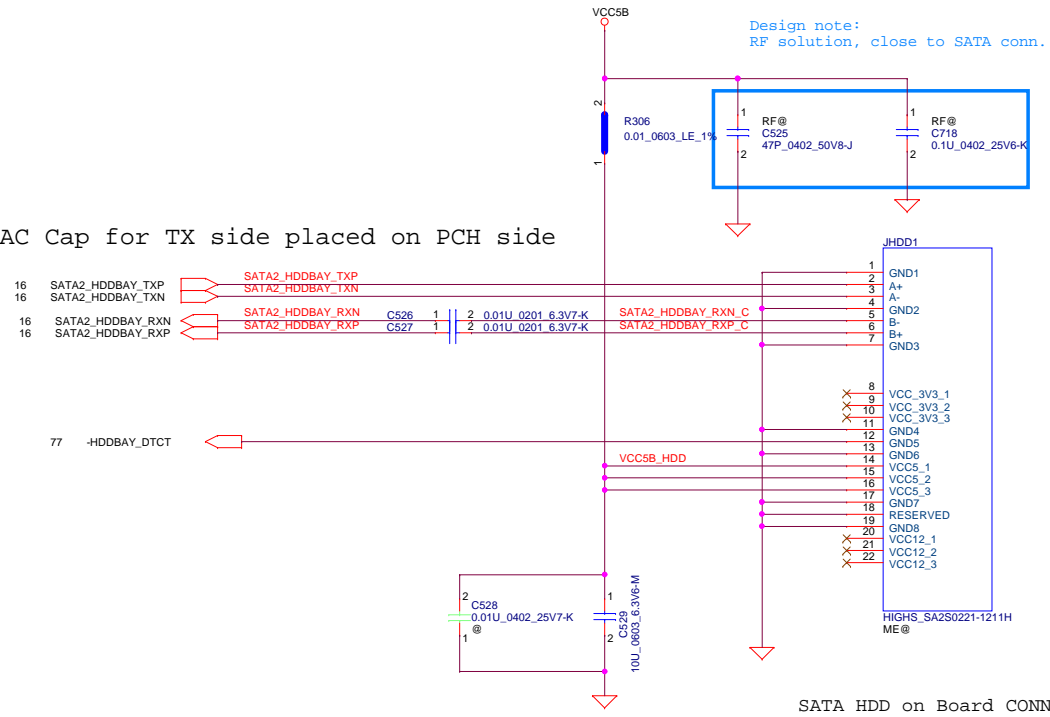


UHS II Interface	UHS I Interface
4 VDD1 3.3V	1 CD/DAT3
7 RCLKP	2 CMD
8 RCLKM	3 VSS1
10 VSS3	4 VDD 3.3V
11 D0P	5 CLK
12 D0M	6 VSS2
13 VSS4	7 DAT0
14 VDD2 1.8V	8 DAT1
15 D1M	9 DAT2
16 D1P	
17 VSS5	



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Issued Date		2015/07/16		Deciphered Date			2016/01/16		SMART CARD READER	
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							Custom	PAYTON	0.1	
							Date:	Wednesday, December 07, 2016		Sheet 64 of 111

AC Cap for TX side placed on PCH side



SATA HDD on Board CONN

Security Classification	LC Future Center Secret Data		Title	SATA HDD CONN	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	Size	Document Number
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			Date:	Wednesday, December 07, 2016	Sheet 65 of 111

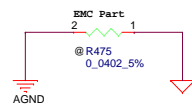
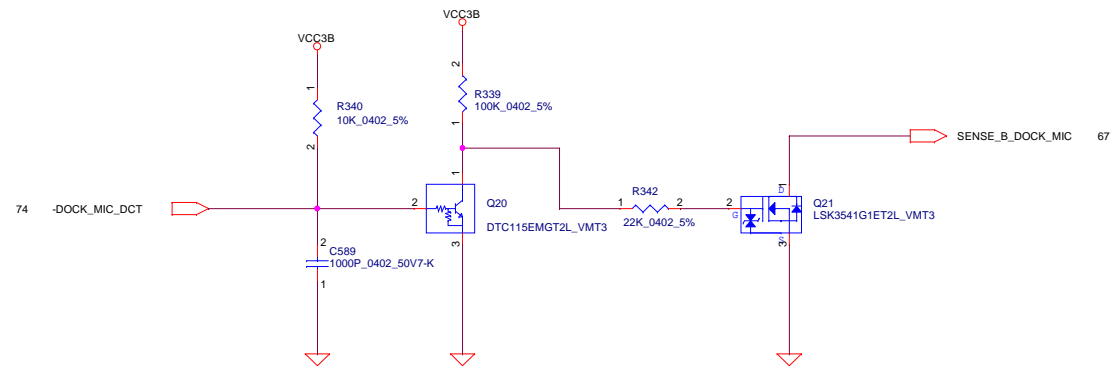
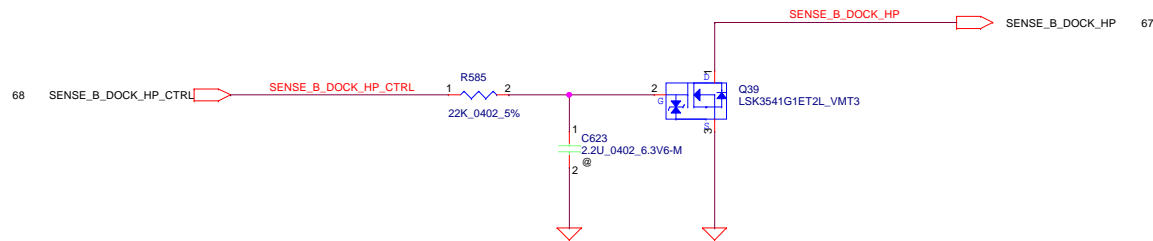
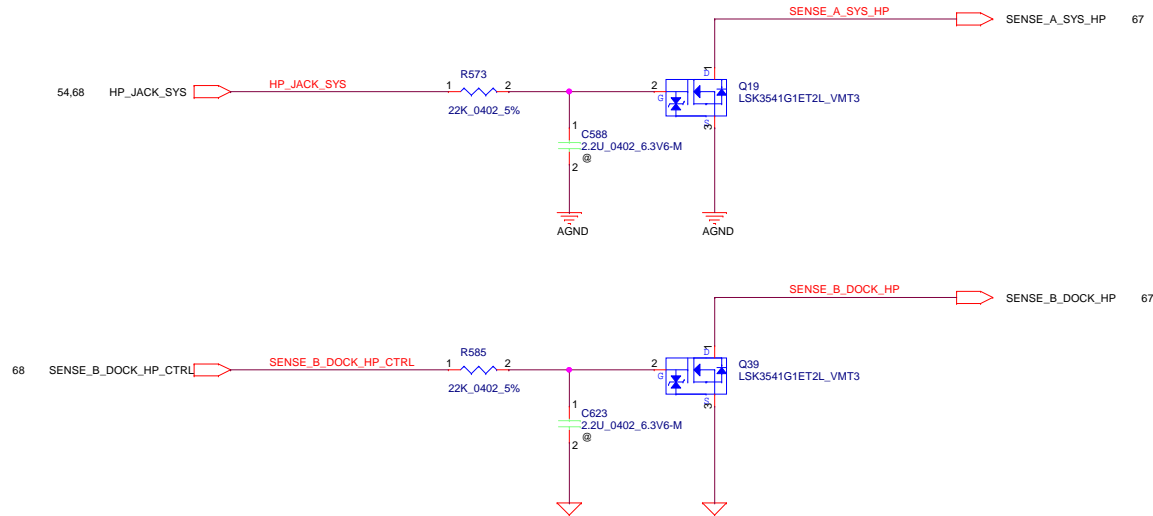


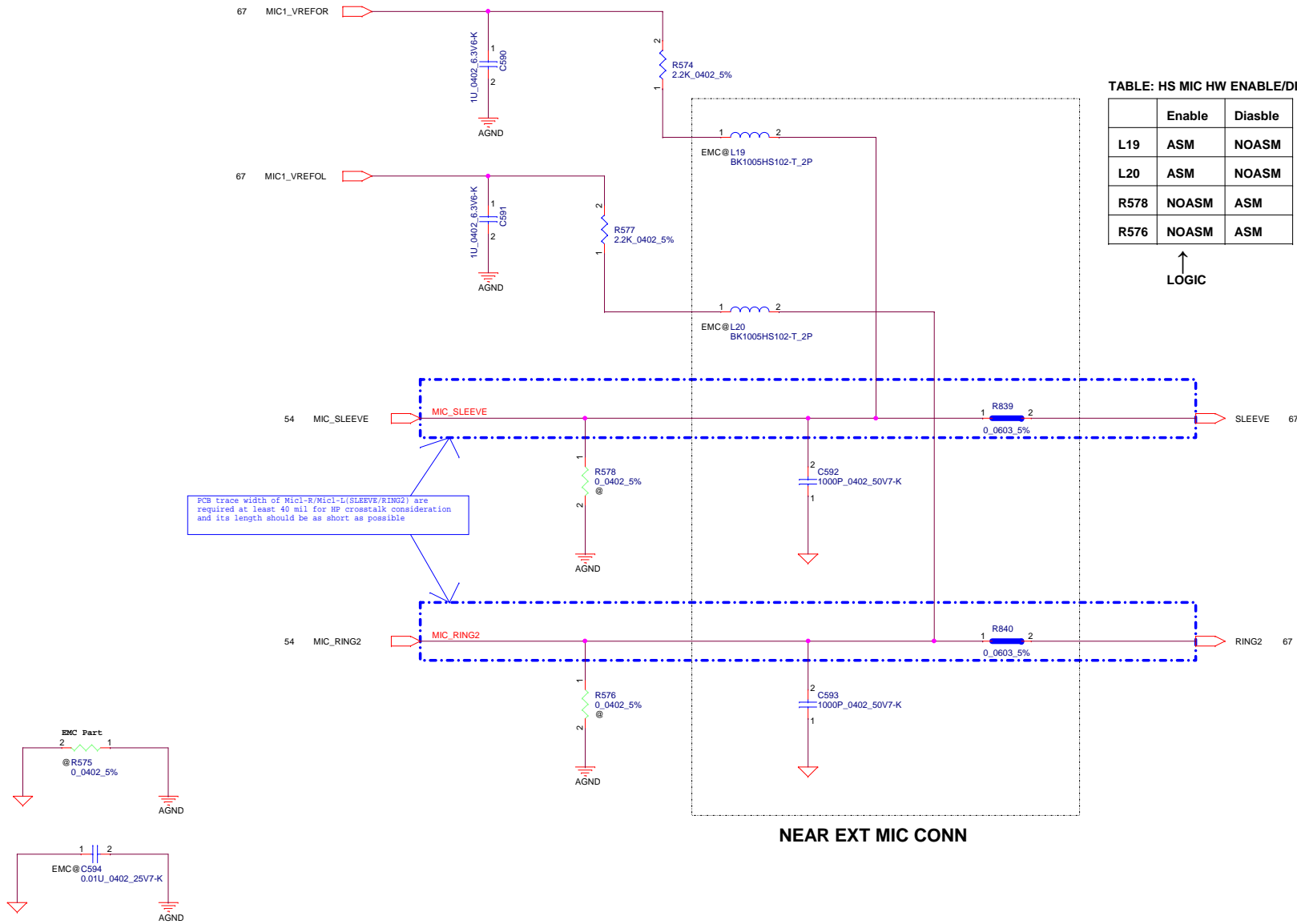


TABLE: DOCK MIC HW ENABLE/DISABLE

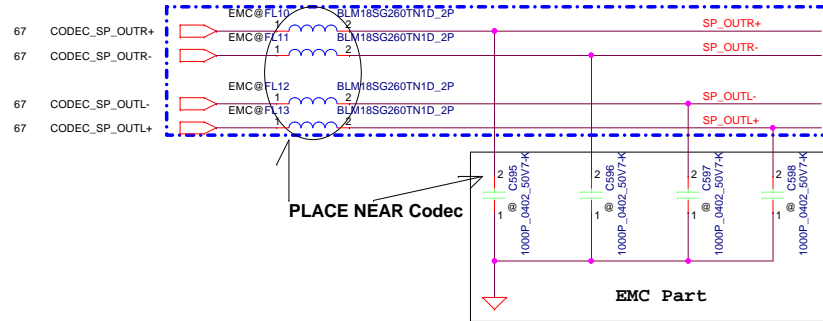
	Enable	Disasble
R340	ASM	NOASM
R446	ASM	NOASM
R339	ASM	NOASM
Q20	ASM	NOASM
R342	ASM	NOASM
Q21	ASM	NOASM

↑
LOGIC

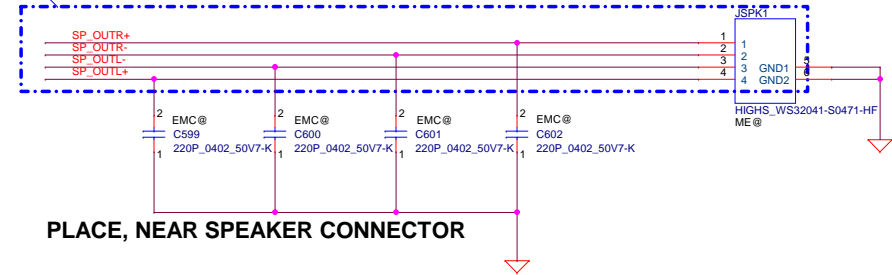




ALC3268 speaker output part

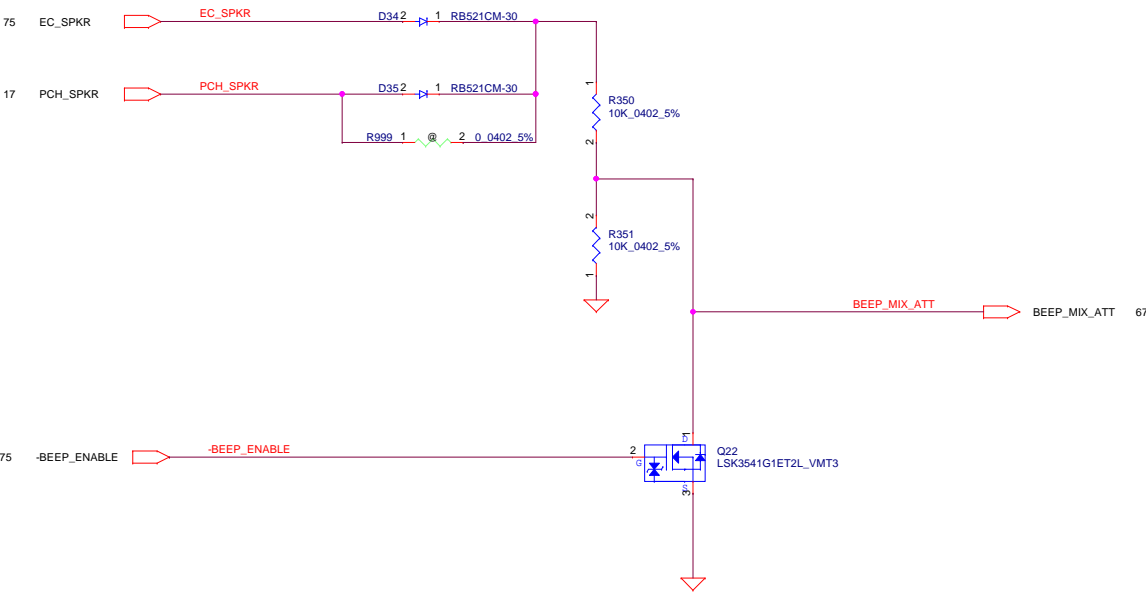




Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

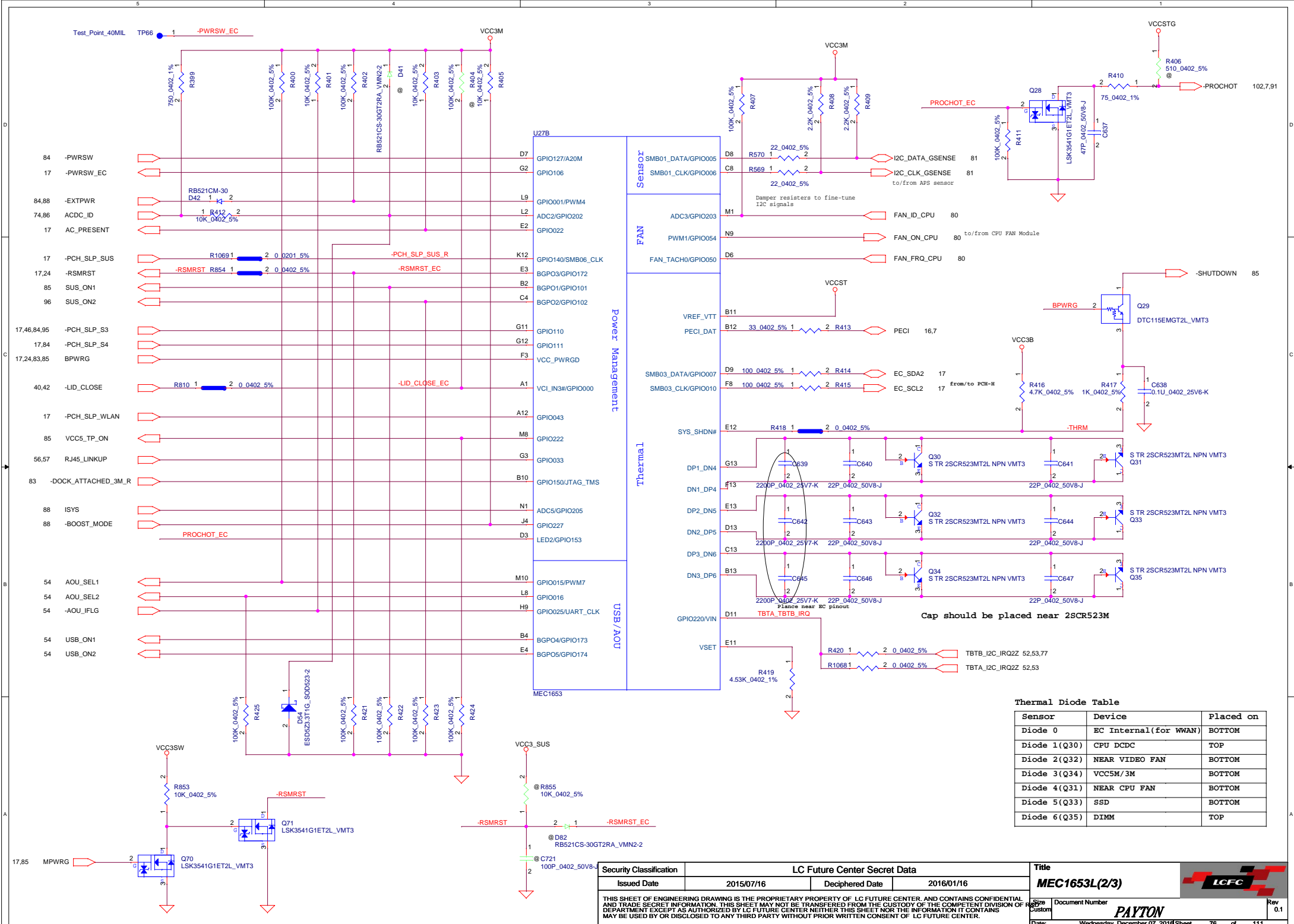


Security Classification	LC Future Center Secret Data		Title	AUDIO SPEAKER	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	Size	Document Number
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				Date:	Wednesday, December 07, 2016
				Sheet	71 of 111
				Rev	0.1

D34 for Enhanced PC Beep function.
No use mount R999, unmount D34, D35

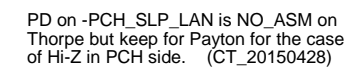


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Issued Date	2015/07/16	Deciphered Date	2016/01/16	SMART AMP					
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				Custom					
				Date:	Wednesday, December 07, 2016	Sheet	73	of	111

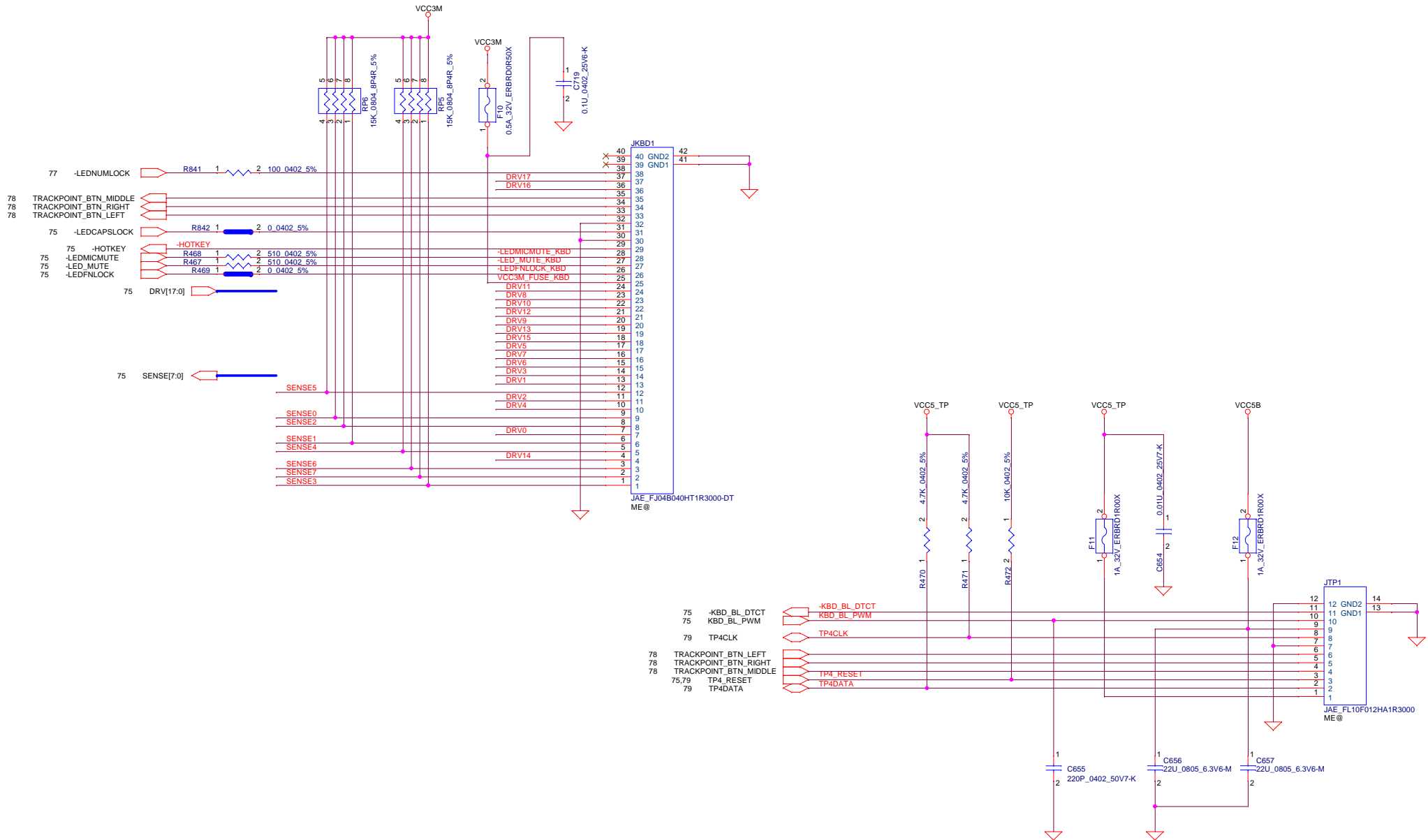


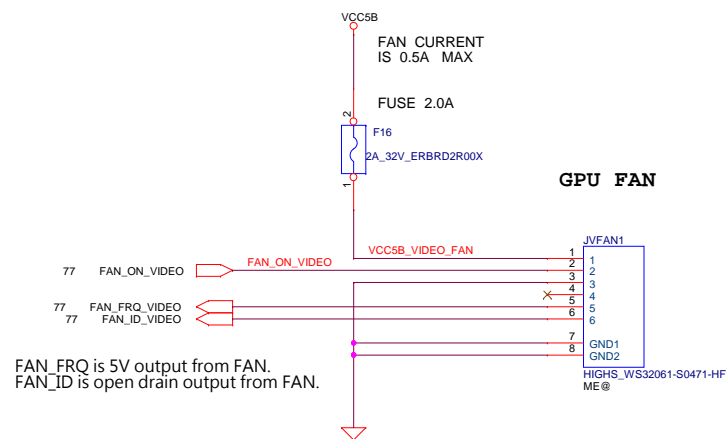
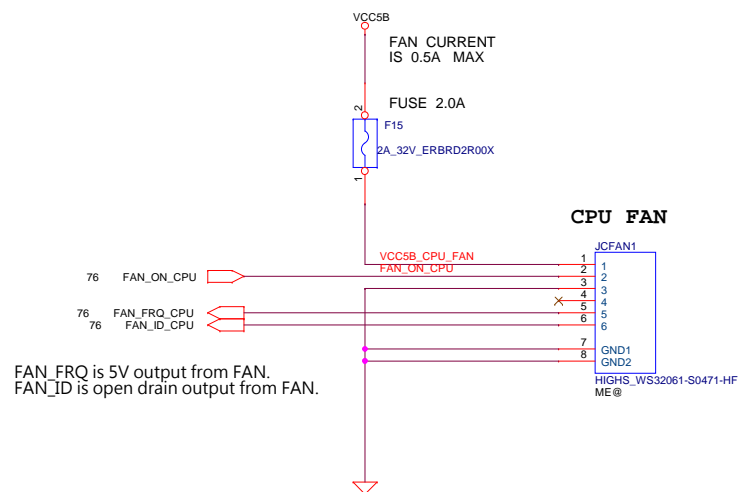
Thermal Diode Table

Sensor	Device	Placed on
Diode 0	EC Internal(for WWAN)	BOTTOM
Diode 1(Q30)	CPU DCDC	TOP
Diode 2(Q32)	NEAR VIDEO FAN	BOTTOM
Diode 3(Q34)	VCC5M/3M	BOTTOM
Diode 4(Q31)	NEAR CPU FAN	BOTTOM
Diode 5(Q33)	SSD	BOTTOM
Diode 6(Q35)	DIMM	TOP



Title	MEC1653L(3/3)		
	Size Custom	Document Number <i>PAYTON</i>	
Date:	Wednesday, December 07 2010 Sheet 77 of 111		



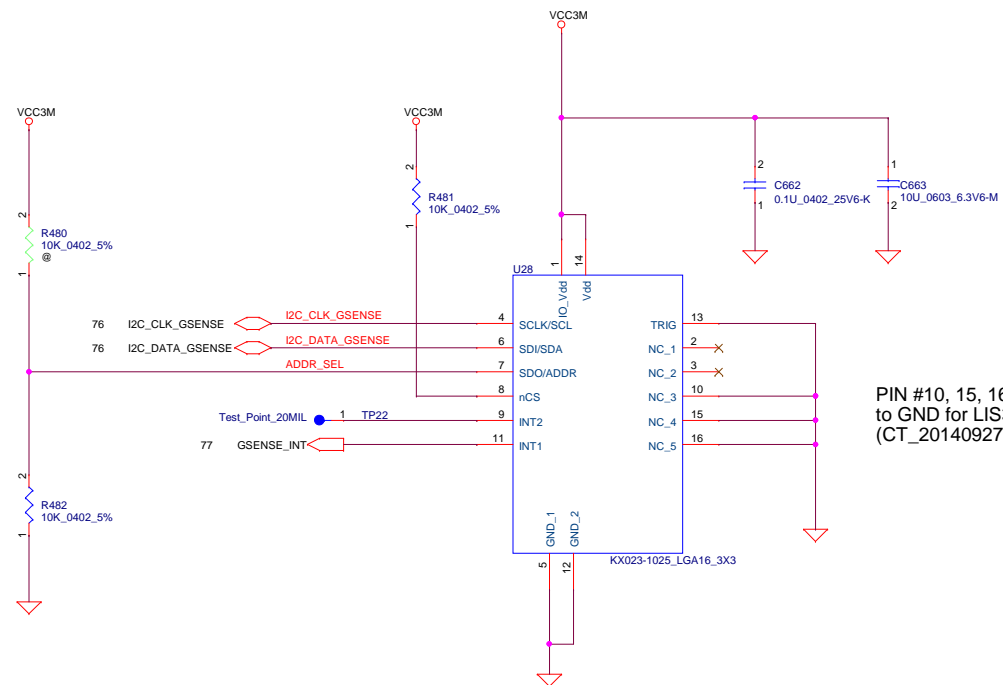


TABLE

P/N	ADDR_SEL	Address
LIS3DH	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

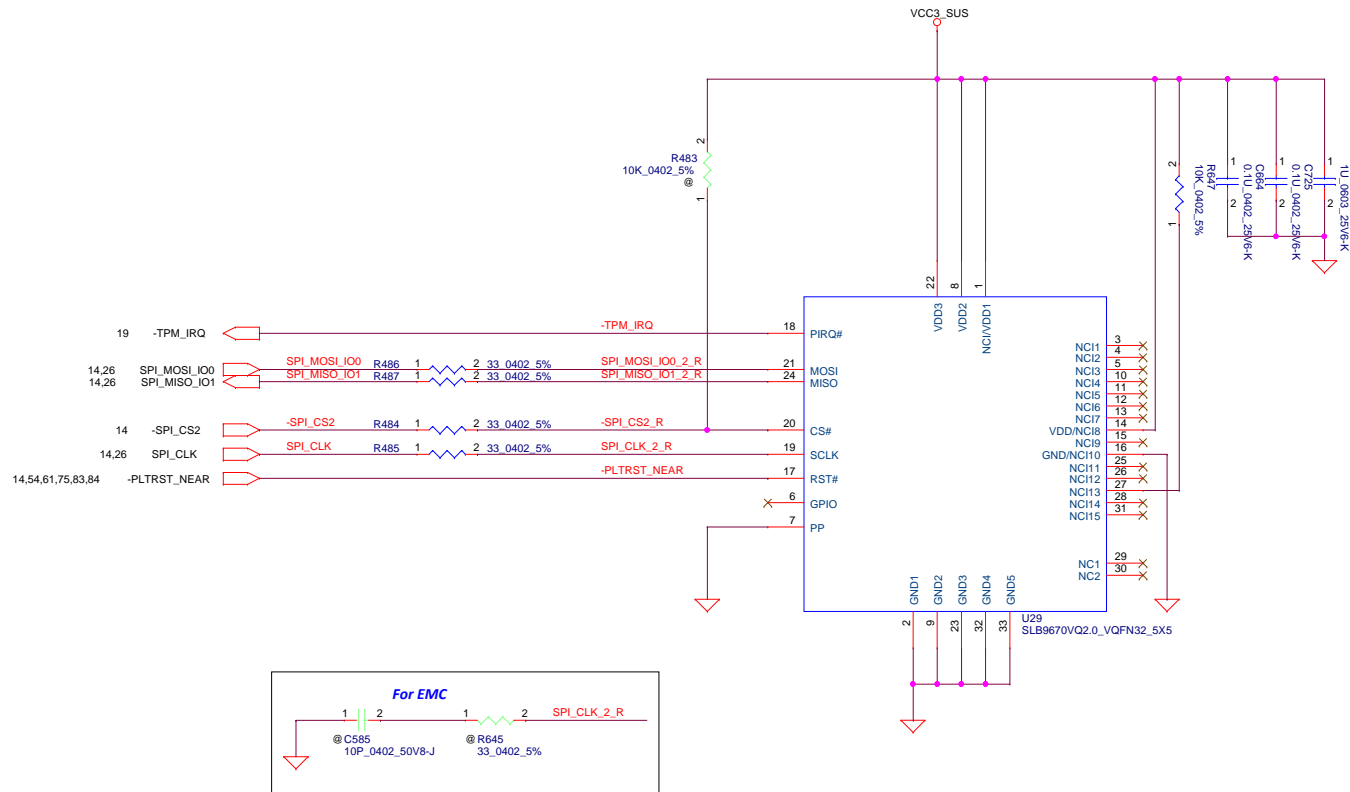


PIN #10, 15, 16 should be connected to GND for LIS3DH. (CT_20140927)

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Title		G-SENSOR	
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Custom			
Date:	Wednesday, December 07, 2016	Sheet	81 of 111



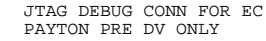


TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0	ST ST33HTPH2E32AAE6
1	VDD	VDD	NIC
2	GND	GND	GND
3	GPIO	NCI	NCI
4	GPIO	NCI	NCI
5	NC	NCI	NCI
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	PP
8	VDD	VDD	NCI
9	GND	GND	NCI
10	VNC	NCI	NCI
11	NC	NCI	NCI
12	NC	NCI	NCI
13	VNC/GPIO	NCI	NCI
14	VDD	NCI/VDD	NCI
15	NC	NCI	NCI
16	GND	NCI/GND	NCI
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VPS
23	GND	GND	NCI
24	MISO	MISO	MISO
25	NC	NCI	NCI
26	NC	NCI	NCI
27	NC	NCI	NCI
28	NC	NCI	NCI
29	VNC/GPIO	NC	NCI
30	VNC/GPIO	NC	NCI
31	VNC	NCI	NCI
32	GND	GND	NCI

Infineon NCI : Not Connected Internally
ST NIC : Not Internally connected

	ENABLE	DISABLE
J30	ASM	NO_ASM
R488	ASM	NO_ASM
R489	ASM	NO_ASM
R490	ASM	NO_ASM
R491	ASM	NO_ASM



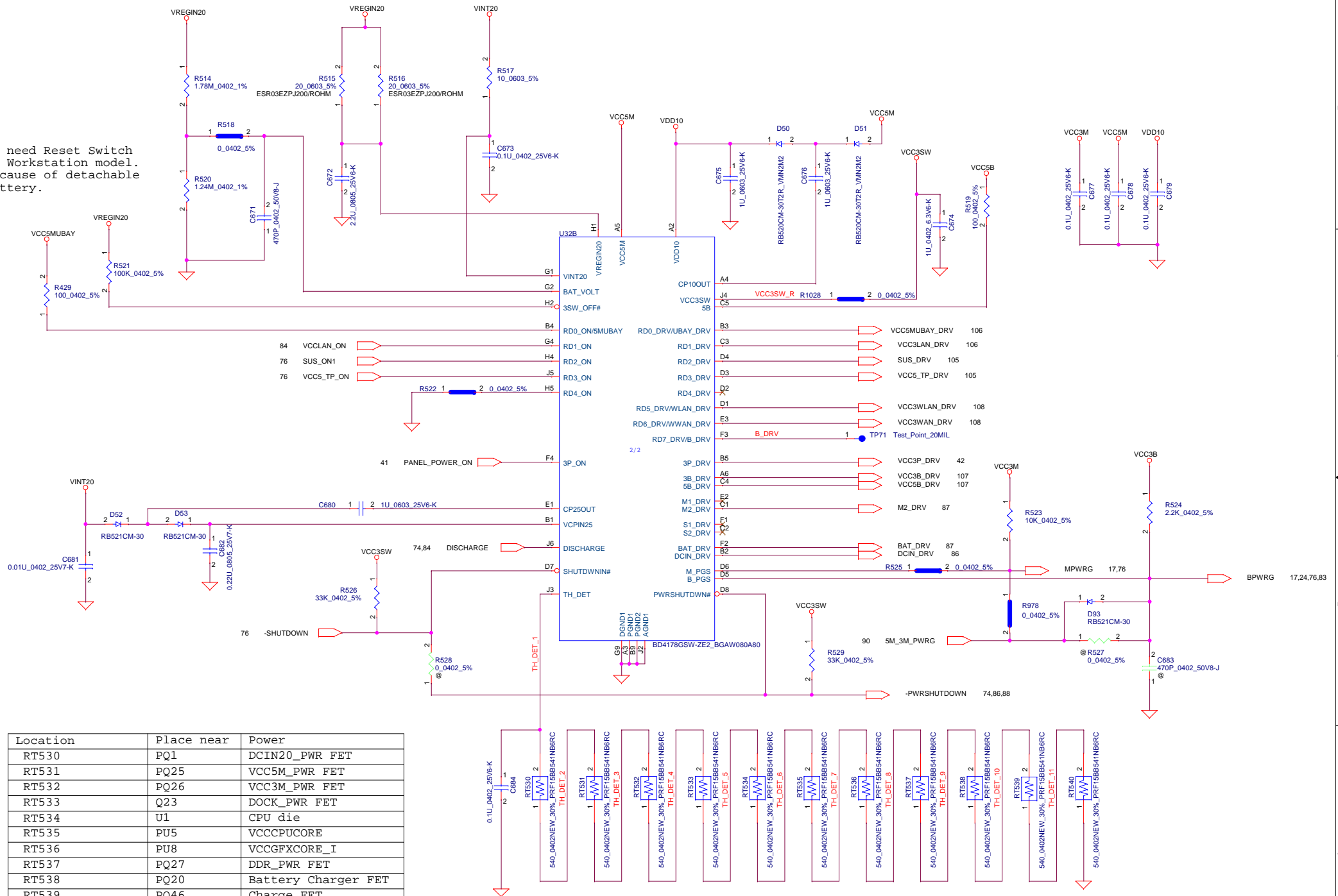
```
Page : 77
JTAG Port Option (JTAG_RST#)
Set to High : Enable
Set to Low : Disable
```

JTAG can work in MHz order

PLACE NEAR EC

Title EEPROM/SMBUS SW			
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No need Reset Switch
on Workstation model.
Because of detachable
battery.



DCIN

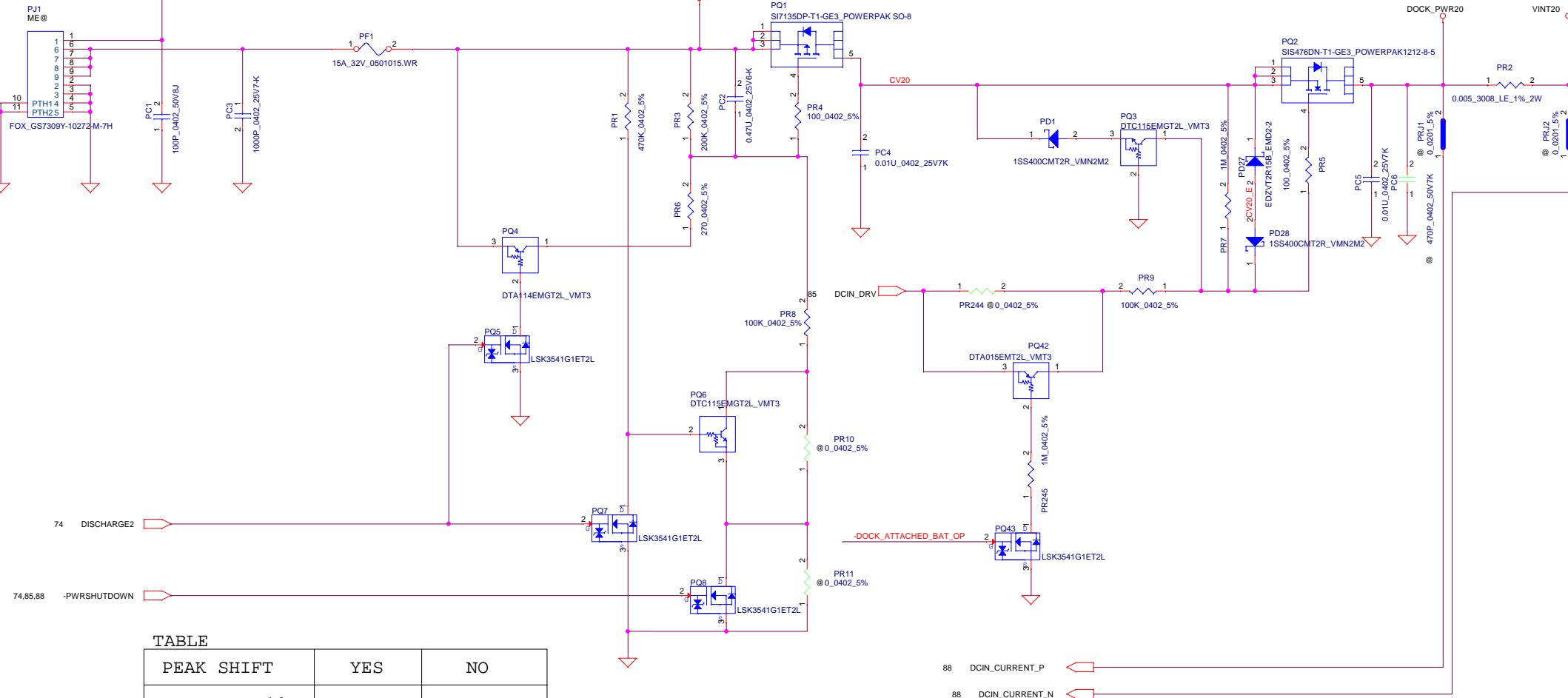
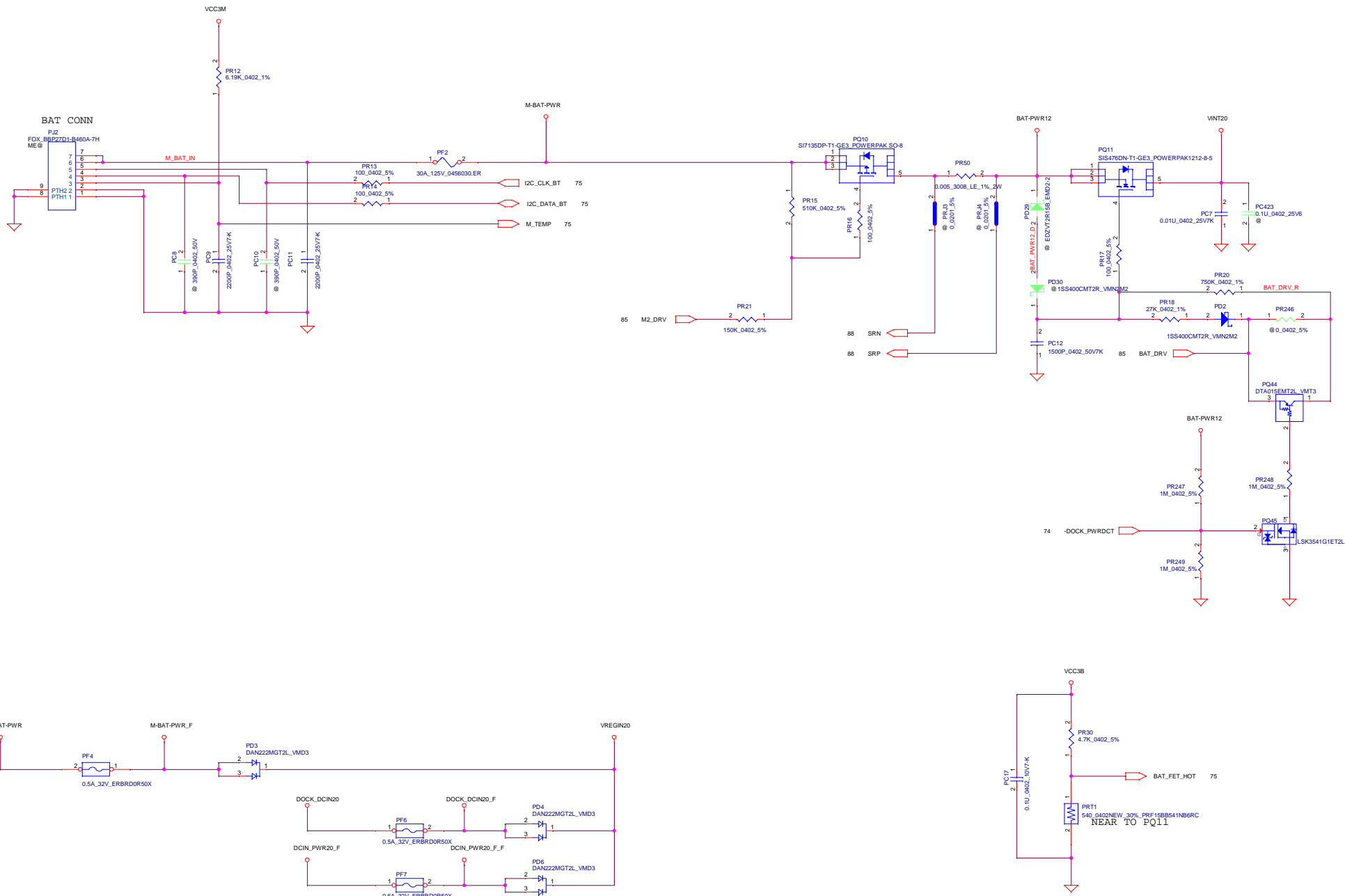
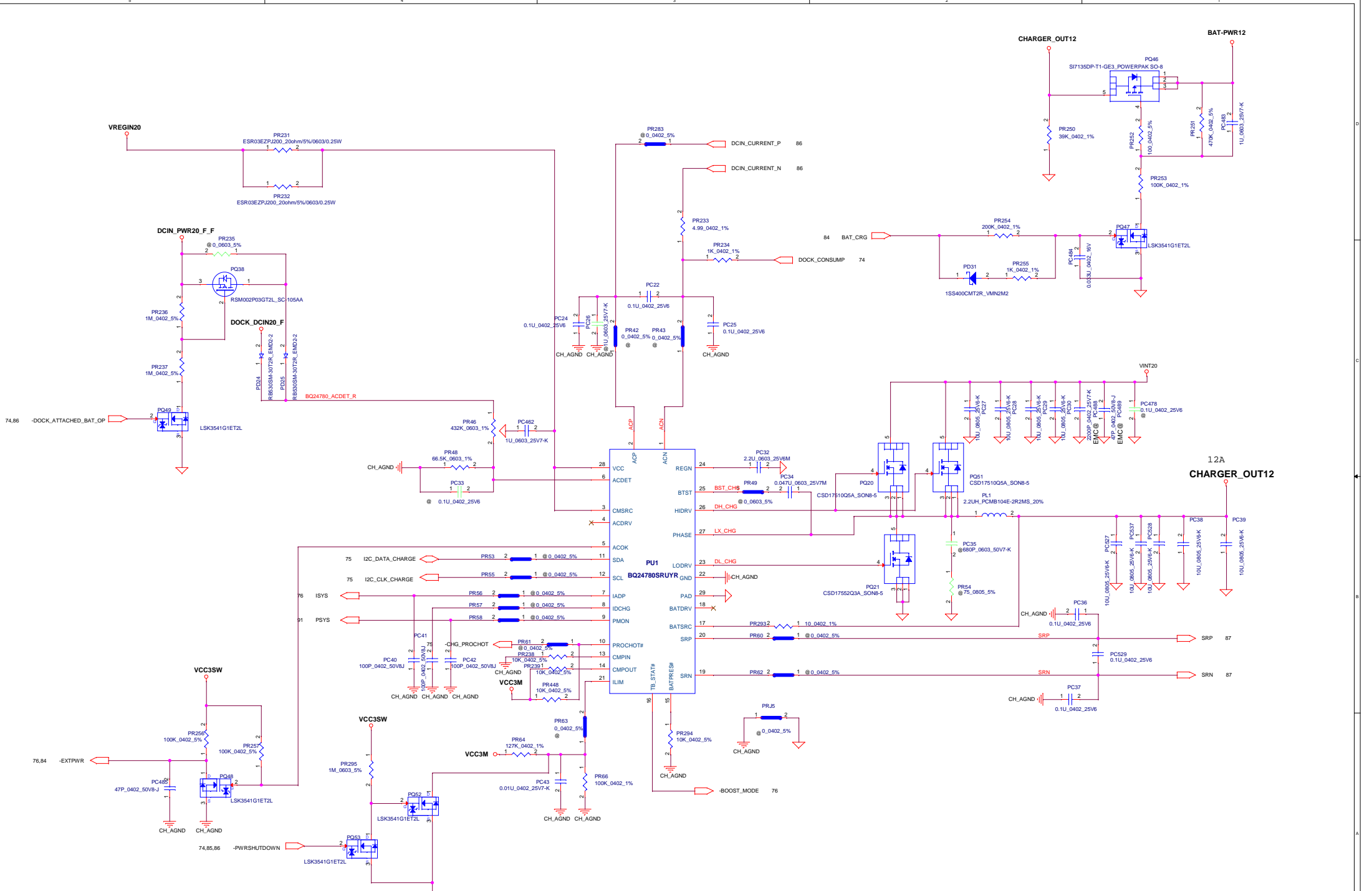


TABLE		
PEAK SHIFT	YES	NO
PR10	NO-ASM	ASM
PR1	ASM	NO-ASM
PQ6	ASM	NO-ASM
PQ7	ASM	NO-ASM


↑
LOGIC

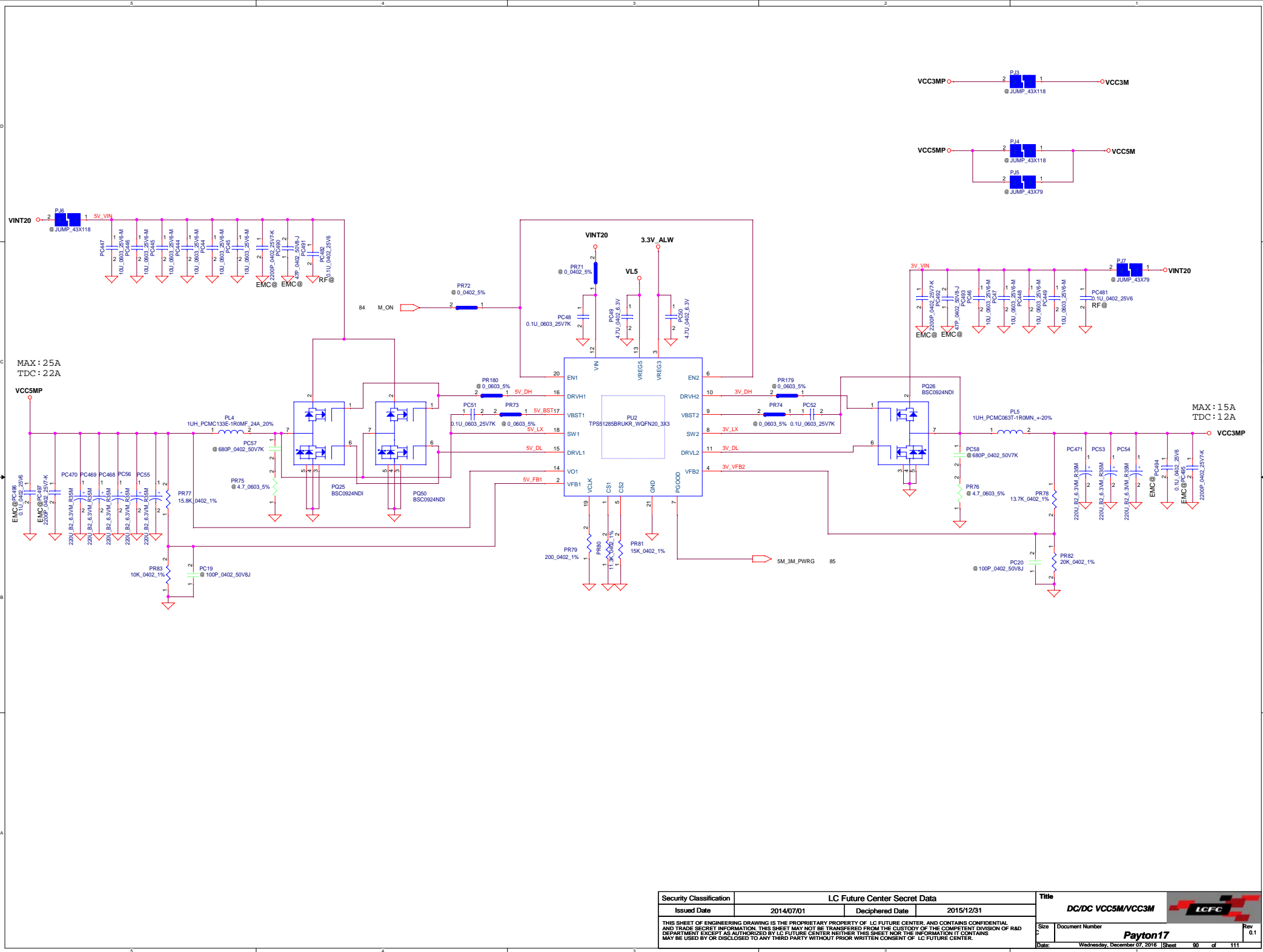


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Date:	Wednesday, December 07, 2016			Sheet	87 of 111

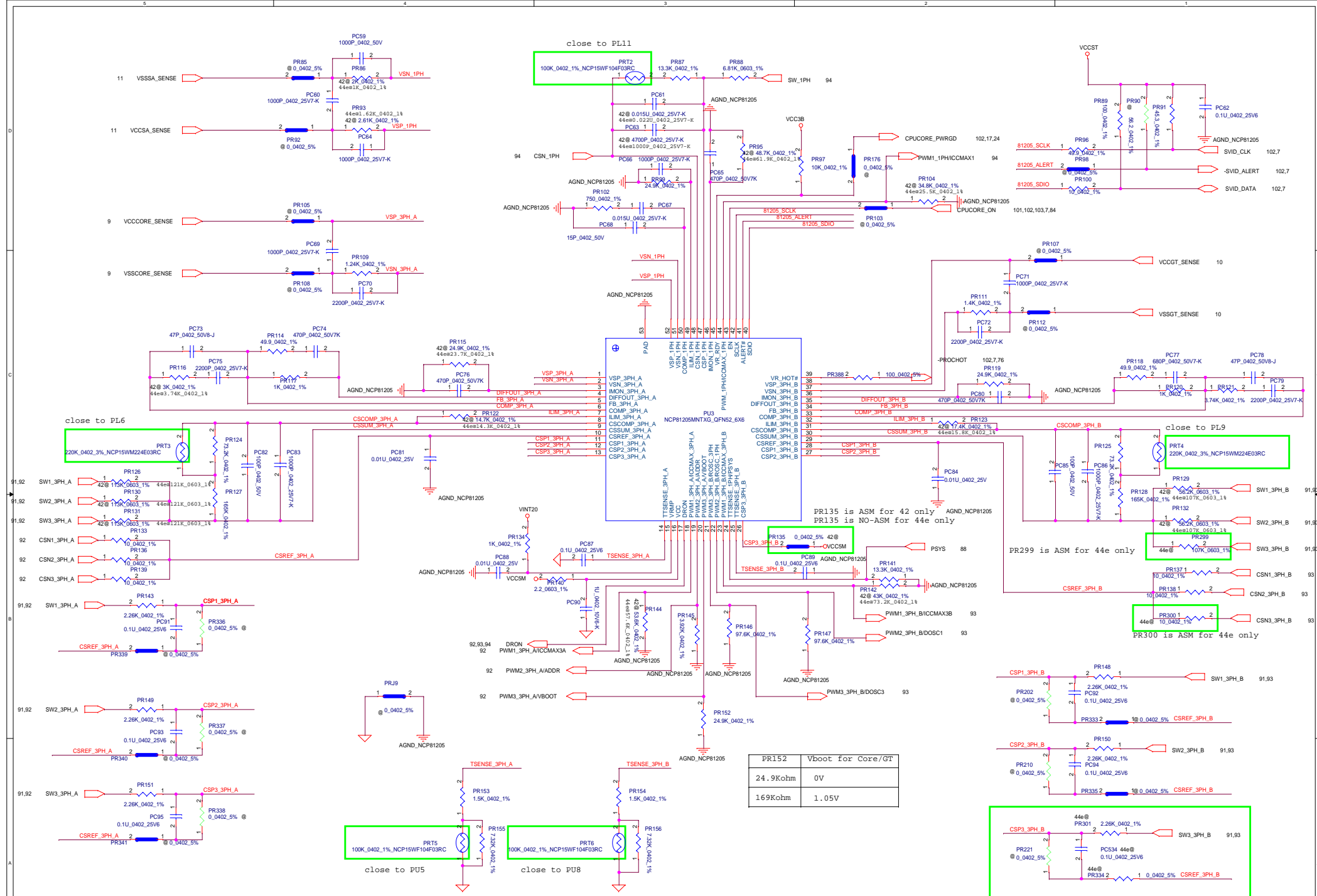


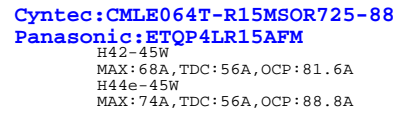
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Issued Date		Deciphered Date		DC/DC VCC5M/VCC3M	
2014/07/01		2015/12/31		Payton17	
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				Rev	
				0.1	
				Date: Wednesday, December 07, 2016	
				Sheet 90 of 111	

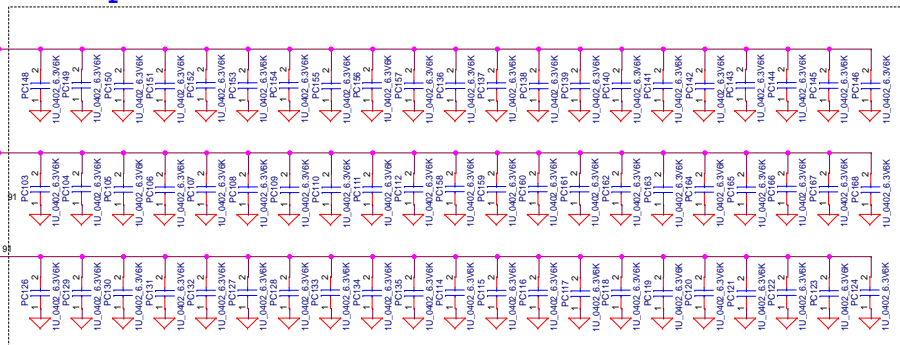


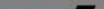


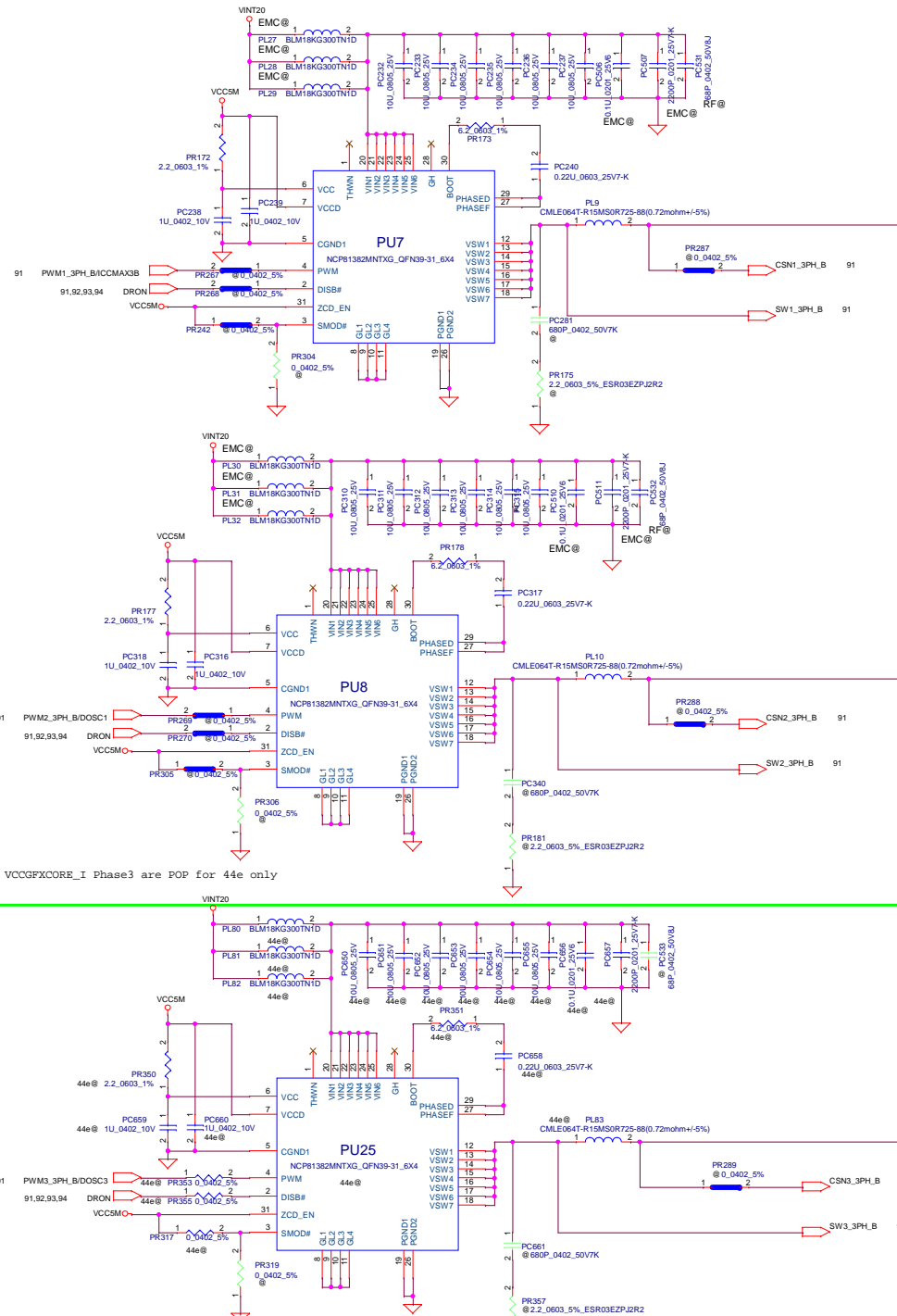
Cyntec:CMLE064T-R15MSOR725-88
Panasonic:ETQP4LR15AFM
H42-45W
MAX:68A,TDC:56A,OCP:81.6A
H44e-45W
MAX:74A,TDC:56A,OCP:88.8A



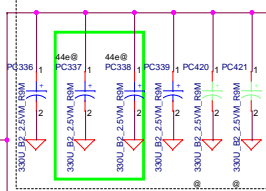
47uF 4pcs



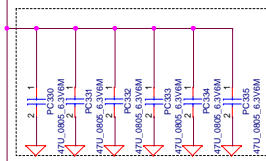
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Issued Date	2014/07/01	Deciphered Date	2015/12/31	DC/DC VCCPUCORE	
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				Date: Wednesday, December 07, 2017 Sheet 92 of 111	Rev 0.1



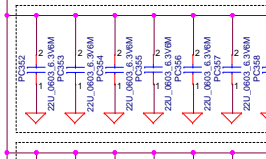
H42-45W
MAX:55A,TDC:39A,OCF:66A
H44e-45W
MAX:94A,TDC:80A,OCF:112.8A



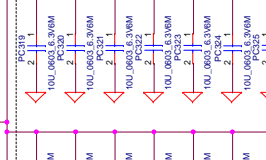
PC337 and PC338 are ASM for 44e only
330uF 4pcs



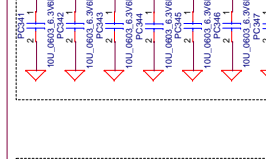
47uF 6pcs



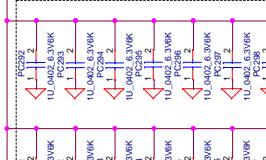
22uF 8pcs



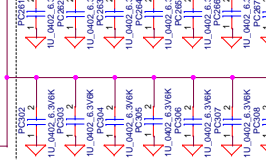
10uF 35pcs



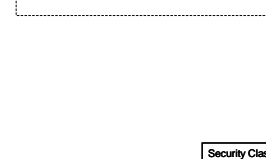
1uF 68pcs



1uF 68pcs



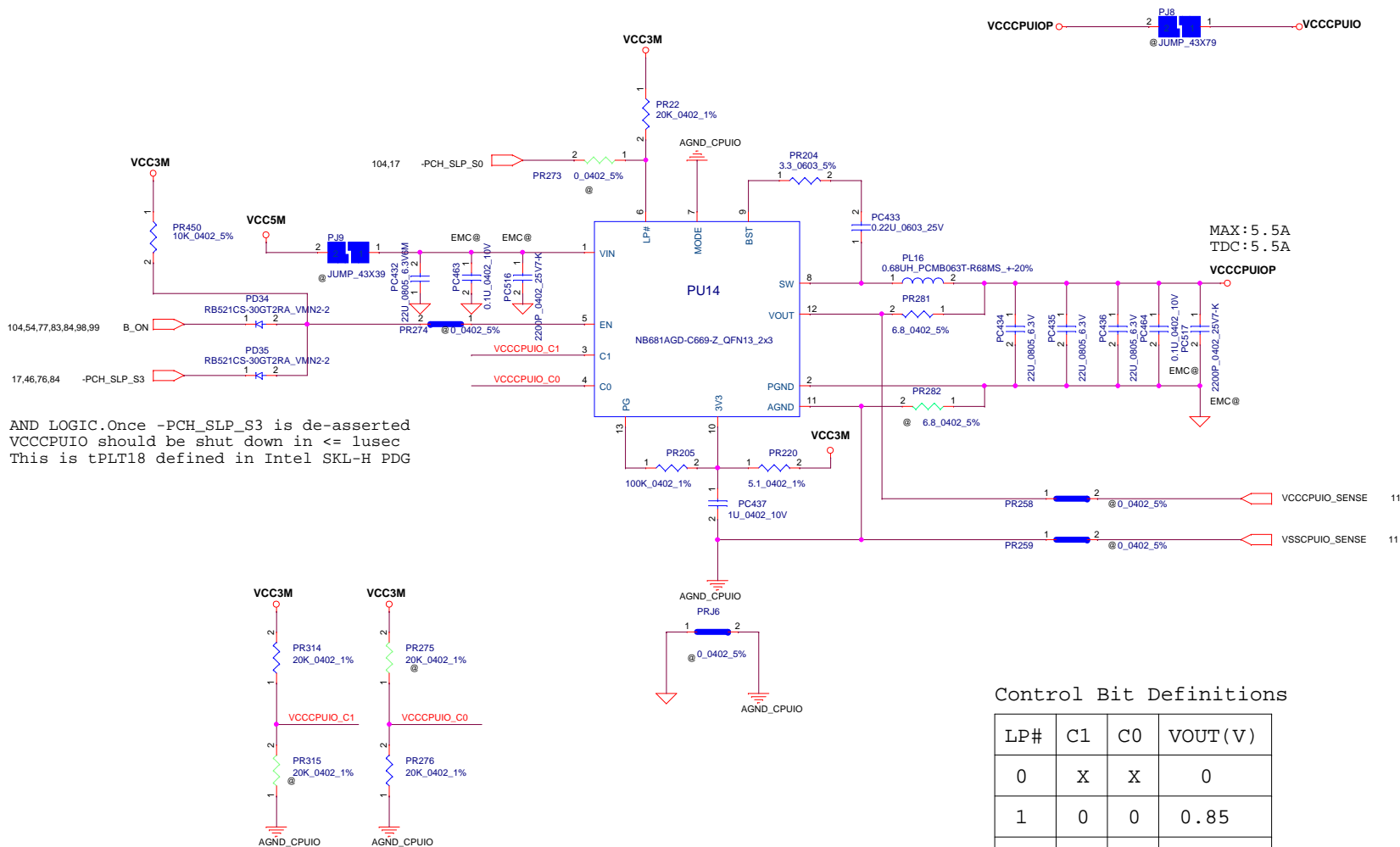
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1uF 68pcs

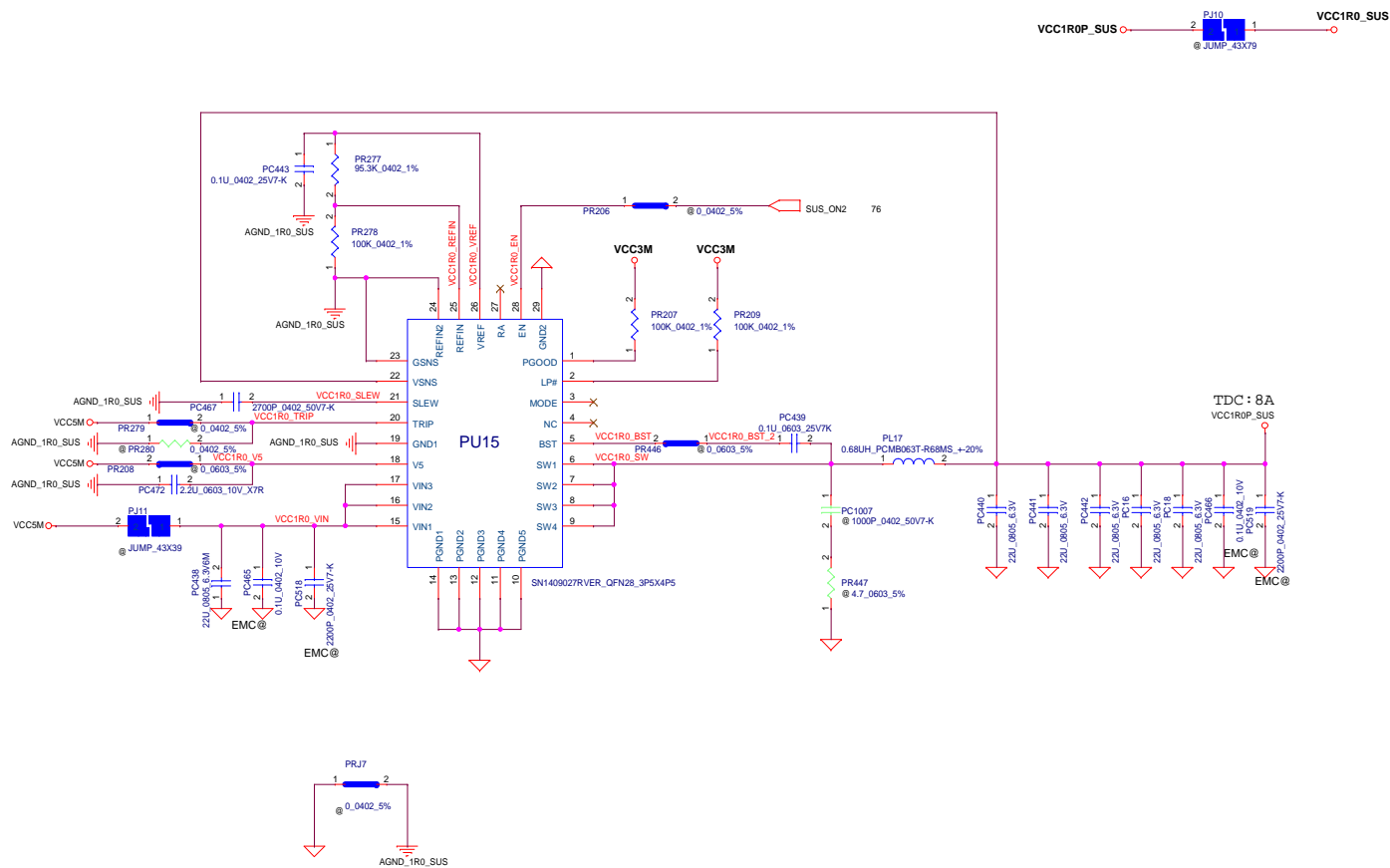
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LC Future Center Secret Data			
Issued Date	2014/07/01	Deciphered Date	2015/12/31
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Document Number	Payton17		
Date	Wednesday, December 07, 2016		
Rev	0.1		

AND LOGIC. Once -PCH_SLP_S3 is de-asserted
VCCCPUIO should be shut down in <= lusec
This is tPLT18 defined in Intel SKL-H PDG




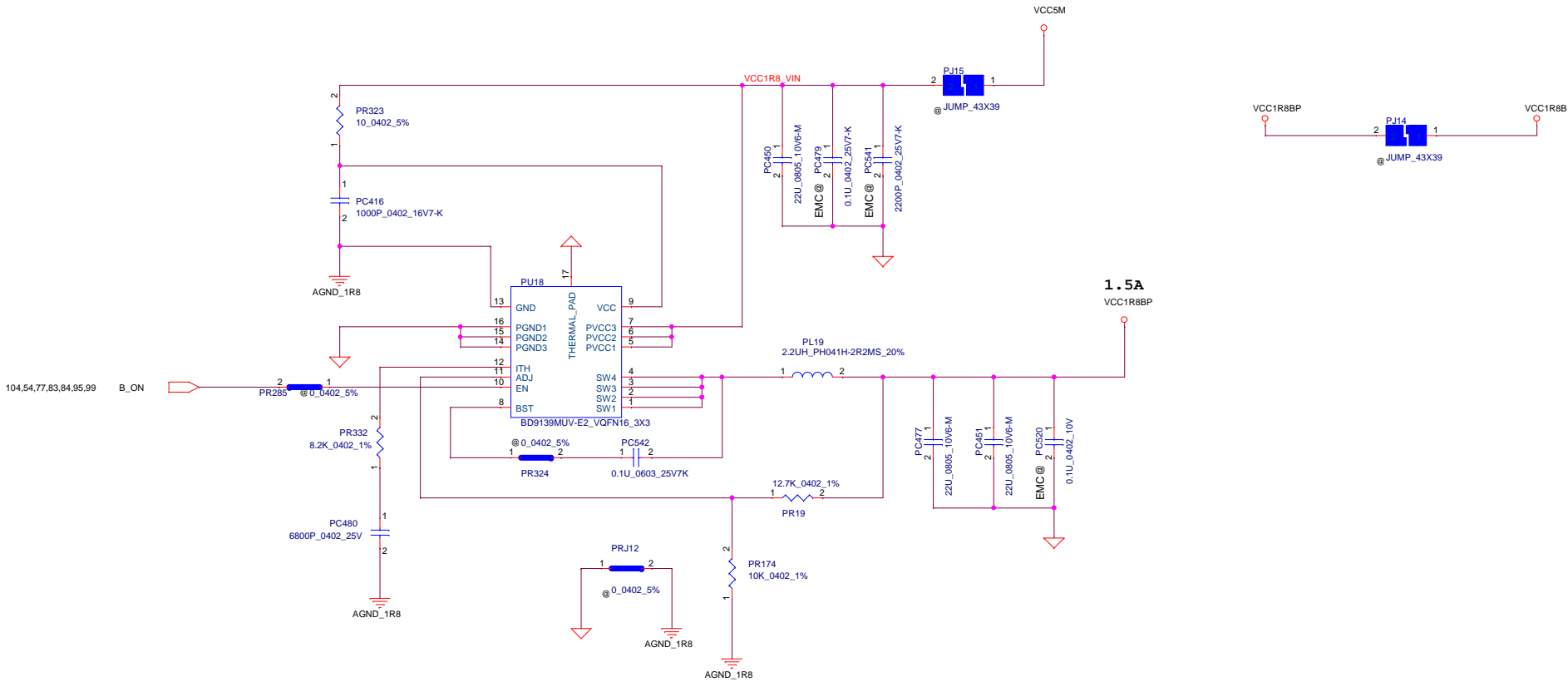
Control Bit Definitions

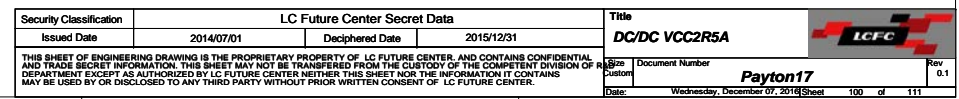
LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
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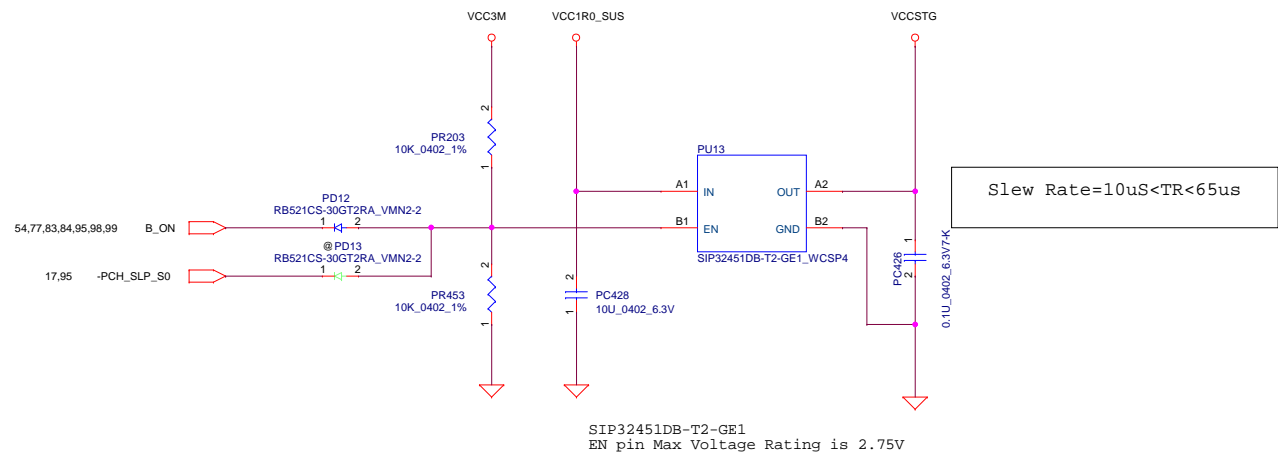
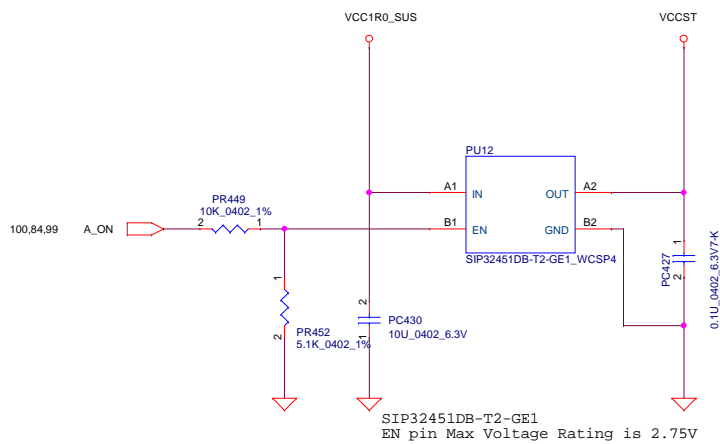


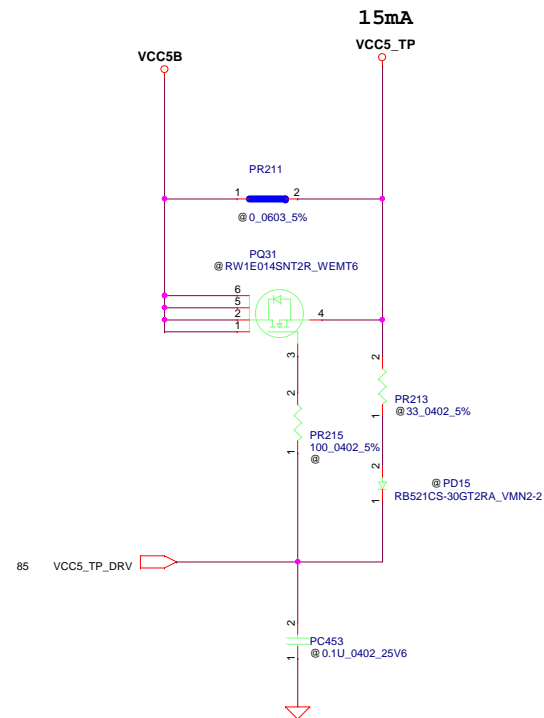
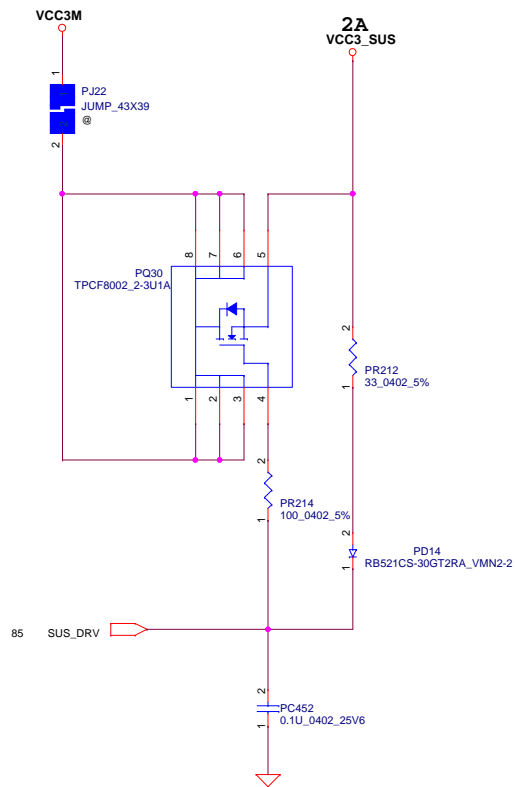
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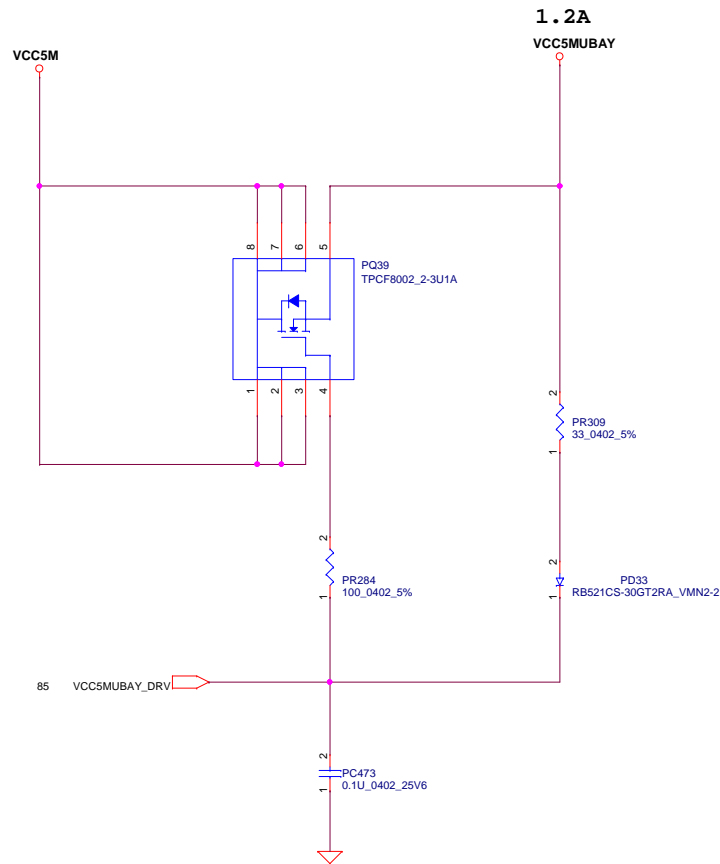
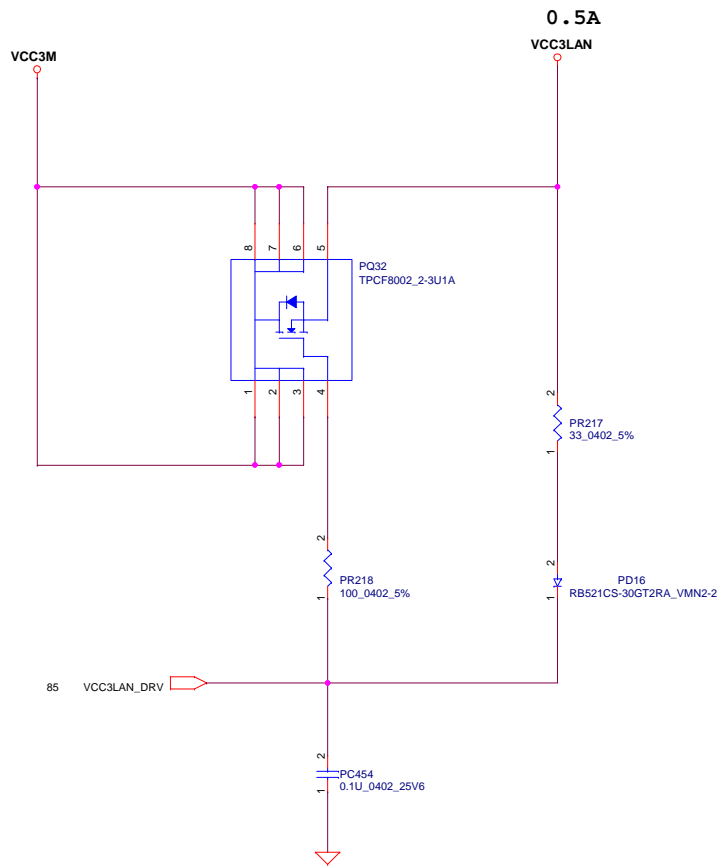
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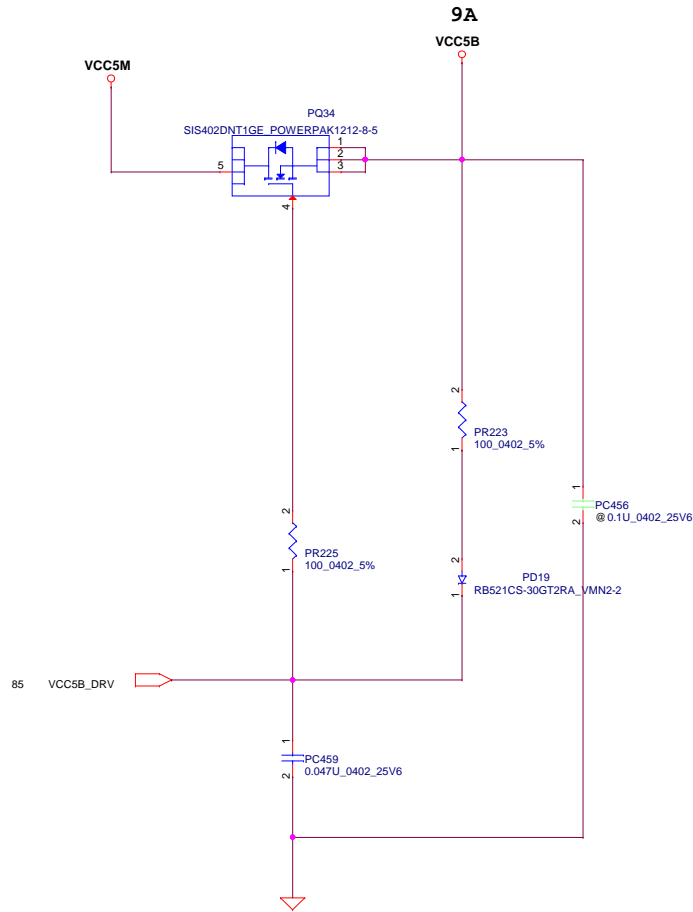
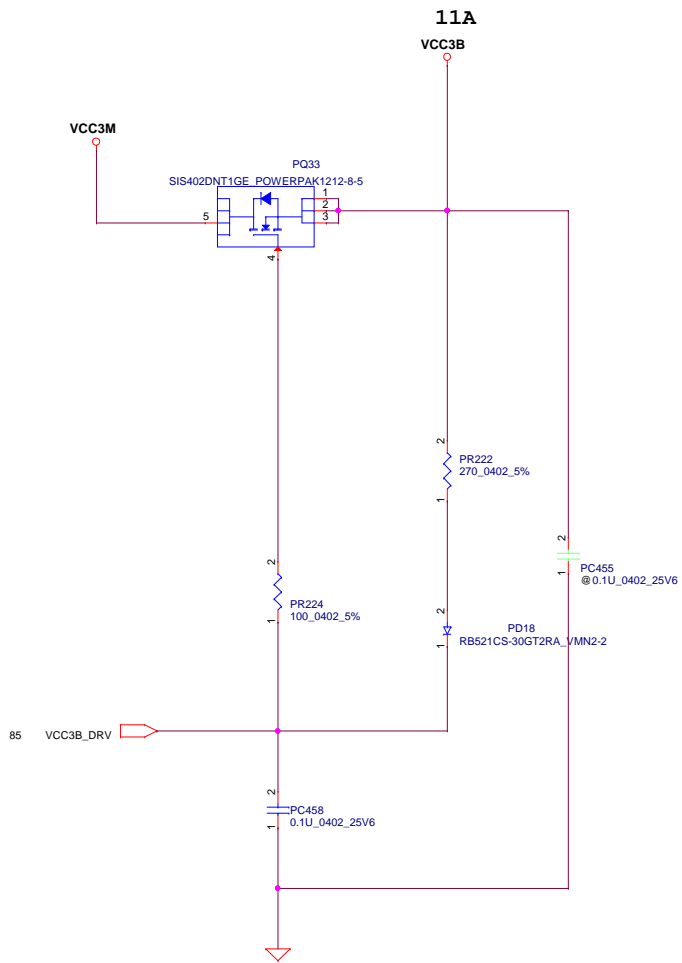
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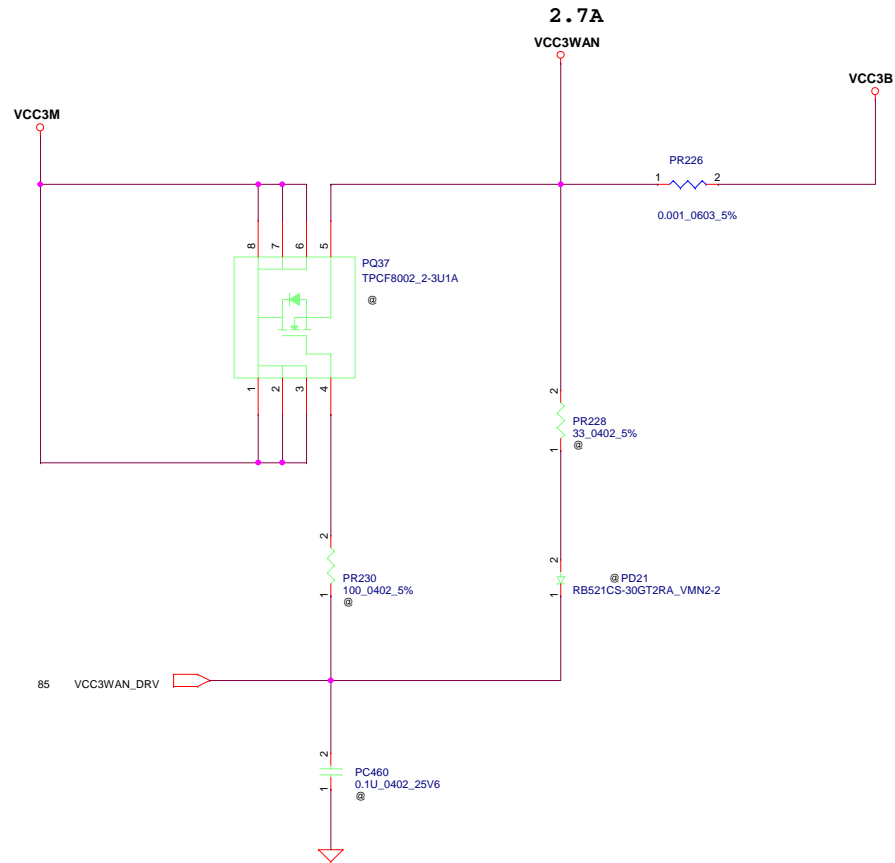
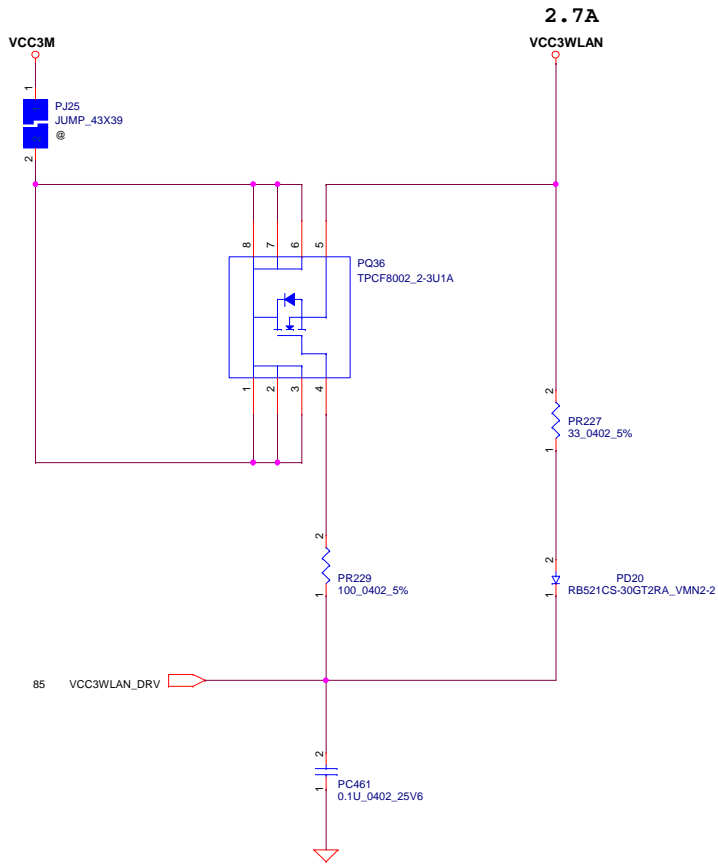
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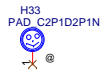
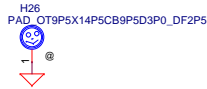
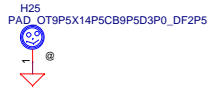
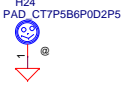




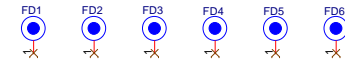








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